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STT-MRAM Cell Reliability Evaluation under Process, Voltage and Temperature (PVT) Variations

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***Abstract*—The CMOS based memories are facing major issues with technology scaling, such as decreased reliability and increased leakage power. A point will be reached when the technology scaling issues will overweight the benefits. For this reason, alternate solutions are being proposed in literature, to possibly replace charge based memories. One of the most promising of these solutions is the spin-transfer-torque magnetic random access memory (STT-MRAM). To evaluate the viability of such solution, one must understand how it behaves under the effect of the various reliability degradation factors. In this paper we propose a methodology which allows for fast reliability evaluation of an STT-MRAM cell under process, voltage, and temperature variations. Our proposed method allows for a sensitivity analysis which will show the designer/test engineer which is the main reliability concern of a certain design. The method is general, and it can be applied to any memory design.**

Keywords—Reliability, Process Variation, Voltage Variation, Temperature, STT-MRAM cell, statistical analysis

I. INTRODUCTION

With technology scaling, the short-comings of well-established memory technologies, like SRAM, DRAM, and flash are becoming more and more difficult to deal with. In the same time, it is harder and harder to design them in such a way that the achieved improvements be significant. These issues have promoted an increased interest in new memory technologies like Magnetic RAMs (MRAMs). One of the most promising magnetic memory is based on the Spin-Transfer-Torque (STT) phenomenon, due to its high speed, high endurance, low area, low power consumption, and good scaling capability [1], especially when it is designed with out-of-plane magnetization. This type of memory features faster read and write access time and better CMOS integration than other available technologies with similar features. However, the STT-MRAM cell fabrication is facing a set of challenges that impact performance and reliability. These issues are related to process variations of MOS and MTJ devices ([2][3][4][5]), to changes in the environmental temperature and to the thermal fluctuations in the MTJ switching ([6]) and to variations in the control voltages. In this paper we propose a reliability analysis of one STT-MRAM cell simultaneously affected by process, voltage and temperature (PVT) variations.

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In the recent years, effort has been dedicated to the evaluation of STT-MRAM cell reliability and the implementation of reliability enhancement techniques. For instance, [7] proposes a classification of STT-MRAM failures based on their physical characteristics, in 'soft failures' (due to stochastic switching and limited thermal stability) and 'hard failures' (due to oxide barrier breakdown and oxide thickness variability), based on which the week cells can be identified. A statistical modeling of failure events of an STT-MRAM cell under process variability is presented in [2]. Here, the failure mechanisms of the MRAM cell are classified and modeled as read failures (decision failure and disturbance failure) and write failure. Robustness metrics for cell evaluation have been proposed in [8]. These metrics provide a way to estimate the extreme parameter variations causing a cell failure, current noise margins and cell failure probability (when failures are observed). In [9] the effect of process and voltage variation on the cell reliability has been investigated, and a power-aware voltage tuning technique for improved STT-MRAM cell reliability has been proposed. For reliability improvement, different techniques have been proposed, like multi-terminal structures [10], new design paradigm decoupling conflicting design requirements between read stability and writability [2], and many others. Circuit-level solutions that enable smaller bit-cell area with improved yield, (bit-line voltage boosting, word-line voltage boosting, access transistor body biasing, and an applied external magnetic field) are proposed in [11].

In this paper, we evaluate the reliability of the STT-MRAM cell under simultaneous effect of process, voltage and temperature (PVT) variation. We estimate the STT-MRAM cell reliability under fabrication- and aging-induced process variability by evaluating its failure probability. This analysis is performed at different supply voltages and different temperatures. The stochastic thermal effect is also evaluated by performing the analysis on bit-cells with different thermal stability coefficients. To the best of our knowledge, this is the first time this type of analysis has been proposed.

The rest of the paper is organized as follows. In Section II, the basic operation principle of an STT-MRAM cell is described. Section III contains a failure analysis of the memory cell, based on its electrical characteristic, including a discussion on how variations in the cell supply voltage and environmental temperature can affect the cell functionality margins and reliability. In Section IV, we present the results obtained for cell reliability estimated under process variability and aging effects, assuming nominal and non-nominal values

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of the supply voltage and various environmental temperatures. Section V concludes the paper.

II. STT-MRAM CELL-PRINCIPLE OF OPERATION

In Spin-Transfer Torque Magnetic Random Access Memories (STT-MRAMs), information is stored into devices called Magnetic Tunneling Junction (MTJ). An MTJ is usually composed of two ferromagnetic layers separated by one oxide barrier. One of the ferromagnetic layers has a pinned magnetization direction (*fixed ferromagnetic* layer), set at fabrication time. The magnetization direction of the second ferromagnetic layer is unpinned (*free ferromagnetic* layer), i.e., it has a freely rotating magnetic orientation that can be dynamically changed by forcing a sufficiently large spin polarized current through the device.

One of the fundamental properties of an electron is that it behaves like a tiny magnet, i.e., it has a magnetic dipole moment which comes from its quantum mechanical spin. Due to its quantum nature, the spin of the electron can be in one of only two states; with the magnetic field either pointing 'up' or 'down' (for any choice of up and down). The spin of the electrons in atoms is the main source of ferromagnetism. When these magnetic dipoles point in the same direction their individually small magnetic fields add together to create a much larger macroscopic field. Only atoms with unpaired spins can have a net magnetic moment, so ferromagnetism only occurs in materials with partially filled electron shells. These unpaired spins tend to align in parallel to an external magnetic field. The Spin-Transfer Torque phenomenon is based on the fact that the spin orientation of a magnetic layer can be modified using spin polarized current. An electrical current is generally un-polarized (half of the electrons are 'spin-up', half are 'spin-down'), however, when it passes through a thick magnetic layer (i.e., the fixed ferromagnetic layer in STT-MRAM) it becomes spin polarized (majority of electrons borrow the polarization direction of the magnetic layer). If this spin-polarized current is directed into a second, thinner magnetic layer (i.e., the free ferromagnetic layer in STT-MRAM), angular momentum can be transferred to this layer. This can excite oscillations or even flip the orientation of the magnet. These are the fundamentals of magnetic storage elements.

The relative Magnetization Directions (MDs) of the two ferromagnetic layers defines the conductance of such a magnetic storage element. This effect is called *Tunneling Magnetoresistance Effect* (TMR), magnetoresitive effect that occurs when two ferromagnets are separated by a thin oxide barrier. If this barrier is thin enough, electrons can tunnel from one layer into another. If the magnetizations are in parallel orientations, it is more likely that electrons will tunnel through the thin oxide layer than if the magnetizations are in anti-parallel orientations (due to the extra energy required for spin flip scattering when the MDs are anti-parallel). The tunneling magnetoresistance effect is characterized by the TMR ratio, defined as the relative resistance change between the two magnetized states. When the magnetization directions of the two layers are parallel, the MTJ device exhibits low electrical resistance (R_L), while when they are anti-parallel, the MTJ device exhibits high electrical resistance (R_H) [1]. The TMR ratio is therefore defined as: $TMR= (R_H – R_L)/R_L$. As shown in Fig. 1(a), the parallel and the anti-parallel relative magnetization directions are conventionally associated with the logic states '0' and '1', respectively.

The electrical resistance of the MTJ device (R_{MTJ}) changes with the voltage drop across the device; the voltage-resistance behavior exhibits a hysteresis characteristic (Fig. 1(c)) [1]. From this characteristic the electrical properties of the MTJ device can be extracted. The device resistance in parallel (R_L) and anti-parallel (R_H) magnetizations are given by the R_{MTJ} values at zero volt bias voltage ($V_{DC}=0V$). From the same hysteresis characteristic, the switching conditions of the relative magnetization can be extracted. When there is a positive voltage drop ($V_{DC}>0$) on the MTJ device in parallel magnetization a current flow is generated (I_{MTJ}) through the device. When this voltage drop is large enough for the current to reach the switching threshold value, the magnetization direction of the free ferromagnetic layer is switched. The relative magnetizations are now anti-parallel. A similar situation is encountered when the MTJ initially in anti-parallel magnetization is negatively biased. The switching conditions for the magnetic states are indicated with blue circles in Fig. 1(c). Here, I_{HL} represents the switching threshold current from anti-parallel to parallel state, while I_{LH} represents the switching threshold current from parallel to anti-parallel state.

Several STT-MRAM cell implementations have been proposed. In this work we target the popular 1T1MTJ structure. In this topology, the memory cell consists of one MTJ device connected to one NMOS transistor in series. The cell is accessed by the corresponding control lines, i.e., Bit Line (BL), Source Line (SL) and Word Line (WL). The equivalent electric circuit is provided in Fig. 1(b). For a write '1' operation (W1), the relative magnetization of the two ferromagnetic layers has to be set to anti-parallel. This is achieved charging the Bit Line (BL) to V_{DD} (power supply voltage) while the Source Line (SL) is grounded. In this way, a current flowing through the MTJ device (I_{MTJ}) form BL to SL is generated. For a write '0' operation (W0), interchanging voltages between BL and SL forces the cell to switch to the parallel state. To perform a read operation, a small voltage is applied to the BL, while the SL is grounded and a current flows through the MTJ device (I_R), proportional to its electrical resistance. If the cell stores '0', i.e., the MTJ is in parallel magnetization, its electrical resistance is low, hence the current (I_{R0}) is high. On the other hand, if the cell stores '1', i.e., the MTJ is in anti-parallel magnetization, its electrical resistance is high, hence the current (I_{R1}) is low. On the hysteresis characteristic in Fig. 1(c), the reading conditions for the two states of the MTJ device are marked with green circles. The data stored by the cell is read by differential sensing, using a Sense Amplifier (SA), as shown in Fig. 1(b), the reading current (I_R) is compared against a reference value (I_{ref}) and a decision is made on the memorized state. There are several ways to generate the required reference current. One option, proposed in [12], is to use as reference one STT-MRAM cell, designed using a pinned MTJ device (i.e. all ferromagnetic layers have their magnetization directions set at fabrication time and cannot be changed by normal electrical operations) whose electrical resistance is equal to the average

value of R_L and R_H. Another option is to use reference cells whose MTJ devices are identical to the ones of the cells to be read [13]. In this configuration, half of the reference cells are set to '1', while the other half are set to '0'. They are configured in such a way that their equivalent resistance (R_e) equals the average of the low and the high resistances of the MTJ devices, i.e., $R_e = (R_H+R_L)/2$.

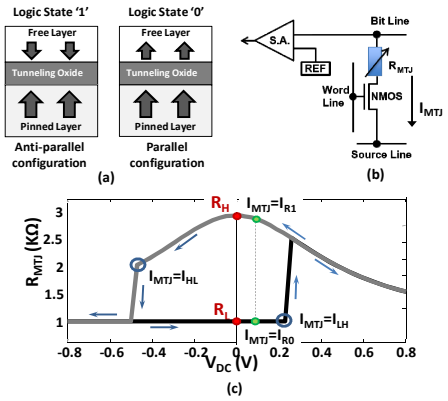

Fig. 1. The STT-RAM Memory cell: a) MTJ configurations; b) Electric circuit of 1T1MTJ structure; c) The $R_{MTJ} - V_{DC}$ hysteresis characteristic.

III. STT-MRAM Reliability Estimation Technique

The electrical resistance of the MTJ device is mainly affected by variations in the tunneling oxide thickness and the cross-section area of the free ferromagnetic layer. These variations result in a spread of R_H and R_L values. In addition, the NMOS transistor may also suffer from process parameter variations, resulting, among others, in variations of its threshold voltage. Under these assumptions, we perform the cell reliability analysis starting from a three dimensional space of parameter variations (R_L, R_H, V_{TH}), and applying the Satisfiability Boundary–Statistical Integration (*SB-SI*) method [14] for failure probability estimation. Even though, in [14], the efficiency of the SB-SI method is demonstrated on an SRAM memory cell, the method is general, and can be applied to any system which can be characterized in its parameter domain. The method is based on identifying the region in the parameter space where the cell operates correctly and then statistically integrating over that region to evaluate the probability of the cell to operate correctly under the assumed variability scenario. Analyzing the correct/faulty response of the cell for different values of the cell parameters the acceptance region in the 3D parameter variation space is obtained as explained in [8] and [9], and summarized below.

To allow for a correct write operation (sufficient current) the high and low values of the MTJ electrical resistance must be below R_{HMAX-W} and R_{LMAX-W}, respectively. During read operation, R_H must be high enough ($>R_{HMIN-R}$) and R_L must be small enough ($<R_{LMAX-R}$) for the current conditions to be satisfied and for the state of the cell to be correctly sensed. The values of these constraints (i.e., R_{HMAX-W}, R_{LMAX-W}, R_{LMAX-R} and R_{HMIN-R}) are dependent on the driving capability of the NMOS transistor. A low value V_{TH} means higher driving capability of the NMOS, which translates into relaxation of read and write operation constraints (R_{HMAX-W}, R_{LMAX-W}, R_{HMIN-R}, and R_{LMAX-R}).

The failure probability of the STT-MRAM cell under read and write failures is evaluated using the SB-SI method in [14]. Here, the failure probability is defined as the probability that the device parameters lay outside the acceptance region (i.e. the cell suffers a read failure - RF or a write failure - WF) and it is given by:

$$P_{RF\&WF} = 1 - \int_0^{\min(R_{LMAX-R},R_{LMAX-W})} \int_{R_{HMIN-R}}^{R_{HMAX-W}} \int_{V_{TH-min}}^{V_{TH-max}} f(R_L, R_H, V_{TH}) dR_L dR_H dV_{TH} \quad (1)$$

with R_{LMAX-R}, R_{LMAX-W}, R_{HMIN-R}, R_{HMAX-W} previously defined, V_{TH-min} and V_{TH-max} the extremes values of the NMOS threshold voltage for correct operation of the STT-MRAM cell, and $f(R_L, R_H, V_{TH})$ the probability density of the joint (cumulative) distribution function defining the statistical distribution of the three parameters.

In addition to fabrication-induced process variability, the STT memory is also affected by aging-induced process variability. The main aging degradation mechanism affecting the *MJT element* is the tunnelling oxide breakdown. The breakdown manifests as a decrease of MTJ resistance under repeated application of voltage pulses. Given that to achieve parallel relative magnetization of MTJ low voltage is required, it is safe to assume that the soft breakdown occurs when the anti-parallel magnetization is enforced. Consequently, we focus our analysis on the time dependent R_H degradation. To characterize the time-dependent dielectric breakdown, the percolation model proposed in [15] is used. The time-dependent anti-parallel state resistance ($R_H(t)$) is described by a Weibull distribution. With this, the time dependent failure probability of the STT-MRAM cell under stress can be estimated by using in (1) the time dependent R_H variation.

The data retention failure (DRF) is a statistical phenomena caused by spontaneous magnetic direction flip during data retention. The MTJ element of an STT-MRAM cell, like all magnetic nanostructures, suffers from thermally activated magnetization reversal, according to Néel-Brown theory. The probability for the magnetization of having flipped after a time *t,* given by the Néel-Brown model [16], is:

$$P_{DRF}(t) = 1 - \exp\left[-\frac{t}{\tau_0} \cdot \exp(-\frac{\Delta E}{k_B T})\right] \quad (2)$$

with τ_0 the attempt time (the inverse of the particle vibration frequency, typical value for magnetic recording: $10^{-9}s$ [17]), k_B is the Boltzmann constant, T is the device temperature and ΔE is the height of the energy barrier between the two magnetization states of the free layer.

In this work, we analyze the behavior of an STT-MRAM cell, designed with perpendicular-anisotropy. The thermal stability of the MTJ device is:

$$\frac{\Delta E}{k_B T} = 70 \quad (3)$$

at room temperature, i.e., T = 300K. For the same device, the thermal stability coefficient is 79.8 at 273K and 62 at 348K.

Assuming that failure due to process variation and failure due to thermal switching are independent events, the overall cell failure probability can be extracted by combining (1) and (3) and it is given by:

$$P_f = 1-(1-P_{RF\&WF})\cdot(1-P_{DRF}) \quad (4)$$

In the next section, the results obtained by evaluating the cell failure probability under the joint effect of process, voltage and temperature variations are described.

IV. STT-MRAM Reliability under PVT Variations

The STT-MRAM operation is directly affected by the fabrication- and aging- induced process variability, the values of the supply voltage (V_{DD}), and by the environmental temperature.

We evaluate the reliability of a 1T-1MTJ STT-MRAM cell with MTJ element characterized by typical nominal R_L=*1kΩ* and R_H=*3kΩ* values at ambient temperature. A 45nm PTM technology NMOS transistor is used, designed with minimum gate length and with a width of *270nm*; its nominal threshold voltage is V_{TH}=*247mV*. The cell switching currents are on the order of *170μA*. The MTJ voltage bias during write operation is equal to the supply voltage, V_{DD}=*1V*. The write and read access times are *30ns*. The following assumptions are made regarding to fabrication-induced parameter variations: they follow Gaussian distributions, with mean values given by nominal parameter values, and standard deviations given by σ_{RL}=*3%*R_L, σ_{RH}=*3%*R_H, *and* σ_{VTH}=*30mV*. The parameter values used for the present analysis are

The cell failure probability is obtained by statistically integrating the joint *probability density function* of the electrical parameters, using (1). For the cell under study, the failure probability due to read and write failures is:

$$P_{RF\&WF} = 1.614\cdot10^{-7}$$

at nominal supply voltage, operating at room temperature (T = 300K). The failure probability due to data retention faults assuming a retention time of 10 years is:

$$P_{DRF} = 1.255\cdot10^{-13}$$

at room temperature (T = 300K). Therefore, the failure probability of the STT-MRAM cell under study, assuming 10 years data retention target and variability induced failure, given by (4), is:

$$P_f = 1.614\cdot10^{-7}$$

In this situation, no aging-induced variability is assumed. However, as we have previously stated, the cell electrical characteristics are affected by repetitive stress. Using this assumption, and modelling the degradation of the anti-parallel resistance under repetitive write operations we evaluate the cell failure probability under the joint effect of fabrication- and aging- induced variability. The obtained failure probability curve is depicted in Fig. 2.

Some interesting facts become apparent when analyzing the failure probability estimation results. The curve can be divided in three regions (Fig. 2): in region 1), the cell reliability degradation is almost insignificant during a large number of operation cycles (~10^{16} under our assumptions), region 2) is a fast transitory region in which the failure probability is fast rising to 1, and in region 3) the cell is nonoperational. The onset of region 2) and its duration characterize the cell resilience to aging-induced process variability. The cell reliability degradation in time is governed by the MTJ time-depended degradation.

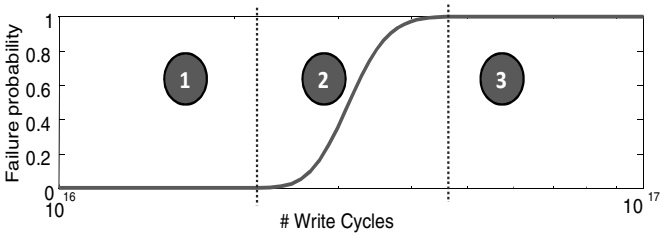

Fig. 2. STT-RAM cell failure probability for cumulative write stress cycles under fabrication- and aging-induced process variability

When evaluating the cell failure probability at different temperatures, the same general behavior is observed, i.e. the cell failure probability is constant for a large number of write operations (~10^{16} write cycles) and relatively small. After this point, the electrical behavior of the cell is relatively degrading, resulting in very high failure probabilities (Fig. 3a). For the "fresh" cell we observe an increase of the failure probability when the device is operating at higher temperatures, i.e., the cell failure probability at T=273K is *2.18·10*$^{-10}$, while at T=348K, the failure probability is *8.24·10*$^{-4}$. This increase is extreme, it shows 6 orders of magnitude reliability degradation in a 75^{o}C operation range. These results are obtained at nominal supply voltage (V_{DD}=1V).

The cell reliability degradation behavior under cumulative write stress, has been evaluated for different values of the supply voltage (Fig. 3b). For the "fresh" cell we observe an increase of the failure probability when the supply voltage decreases, i.e., the cell failure probability when V_{DD}=1.1V is *1.308·10*$^{-11}$, while when V_{DD}=0.9V the failure probability is *0.042*. This increase is extreme, it shows 9 orders of magnitude reliability degradation in a 200mV operation range. These results are obtained at room temperature (T = 273K).

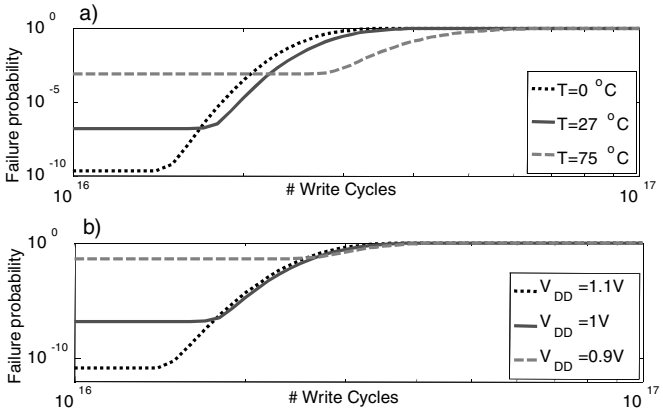

Fig. 3. STT-RAM cell failure probability for cumulative write stress cycles under fabrication- and aging-induced process variability for a) different temperatures of operation; b) different supply voltages.

We observe that the cell electrical behavior is highly sensitive to relatively small changes in temperature an slight variations of the supply voltage. Another observation which can be made regarding the cell reliability, is that the onsets of

device failure due to aging are shifted under supply voltage and temperature variations.

Let's now take a more in-depth look at the cell failure probability at the beginning of its life (Fig. 4a and Fig. 5a), for instance after one write operation ad at the end of life, after $2 \cdot 10^{16}$ write operations (Fig. 4b and Fig. 5b).

When analyzing the effect of temperature variations on the reliability of the fresh cell (Fig. 4a), we observe, as previously stated, a decrease in cell reliability when the operation temperature increases. The same effect is observed when the cell operates at various supply voltages. In Fig. 4a we observe a monotonic behavior of the failure probability with temperature over the whole range of voltages. Also, we observe that the temperature variation effect is lesser as supply voltage increases. If for the cell operating at nominal supply voltage the reliability degradation is of 6 orders of magnitude over a range of 75°C, the reliability degradation is of only 2 orders of magnitude over the same temperature range when the supply voltage is 10% larger than nominal.

Increased temperature causes a decrease in the nominal value of the anti-parallel resistance of the MTJ device, reducing the cell reliability during read operation. In the same time, the thermal stability of the cell decreases. This explains the curves in Fig. 4a). On the other hand, increasing the supply voltage leads to larger currents passing through the MTJ device, resulting in an increased read and write reliability. This effects are competing over temperature and supply voltage variation, and for larger values of supply voltage the detrimental temperature effect is partially compensated by the positive supply voltage contribution.

After repetitive write stress, the reliability of the cell degrades due to the tunneling oxide degradation. When evaluating the cell failure probability after $2 \cdot 10^{16}$ write operations we observe different trends than the ones observed for the fresh cell. In this situation, the failure probability degradation is no longer monotonic with the temperature increase over all supply voltages (Fig. 4b). The monotonic failure probability increase with temperature is observed for large supply voltages, 1.1V and 1.05V in Fig.4b), for which after $2 \cdot 10^{16}$ write operations the cell failure probability is in region 2). When the supply voltage is 1V or 0.95V, after $2 \cdot 10^{16}$ write operations the cell failure probability is either in region 1) or 2) of the failure probability curve, depending on the temperature of operation. This explains the non-monotonic behavior of the reliability curves. For low temperatures, the cell is in region 1) while for high temperatures, the cell is in region 2). It should be noted that the reliability curves in this case have a minimum, which shows the crossing between regions 1) and 2). It is also very interesting to note that the reliability of the cell increases when the temperature increases from 273K to 323K, for V_{DD}=1V, or to 300K for V_{DD}=0.95V. This behavior is contrary to the one observed for the fresh cell. The explanation for this effect can be found analyzing the characteristics of the cell after high repetitive stress. At this point, being very close to the onset of region 2), the cell is very weak, in fact it is weak enough so that temperature increase effect on the access transistor actually makes all the difference on the overall failure probability. Once the cell crosses the boundary into region 2) the degradation of the MTJ becomes dominant and drives the overall cell reliability. When the cell is supplied at V_{DD}=0.9V, after $2 \cdot 10^{16}$ write operations the cell failure probability is in region 1), right before the onset of region 2). The previous discussion applies here too.

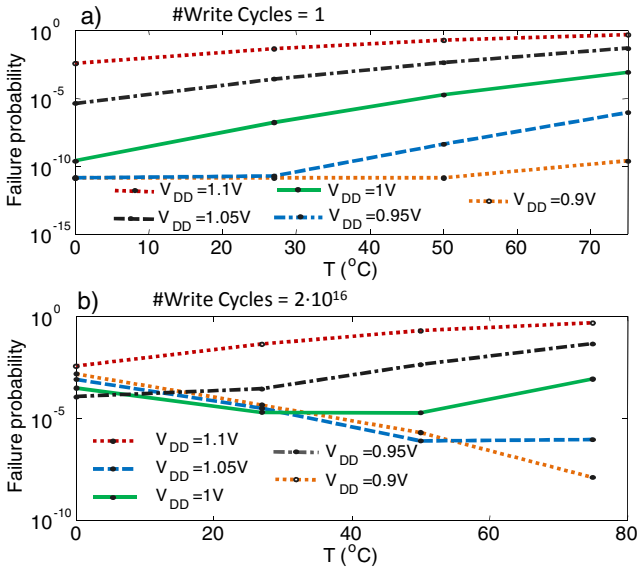

Fig. 4. STT-RAM cell failure probability as function of temperature variation, assuming different supply voltage values, under fabrication- and aging-induced process variability for a) "fresh" cell; b) aged cell

When analyzing the effect of supply variations on the reliability of the fresh cell (Fig. 5a), we observe, as previously stated, an increase in cell reliability when the supply voltage increases. The same effect is observed when the cell operates at various temperatures. In Fig. 5a we observe a monotonic behavior of the failure probability with supply voltage over the whole range of temperatures.

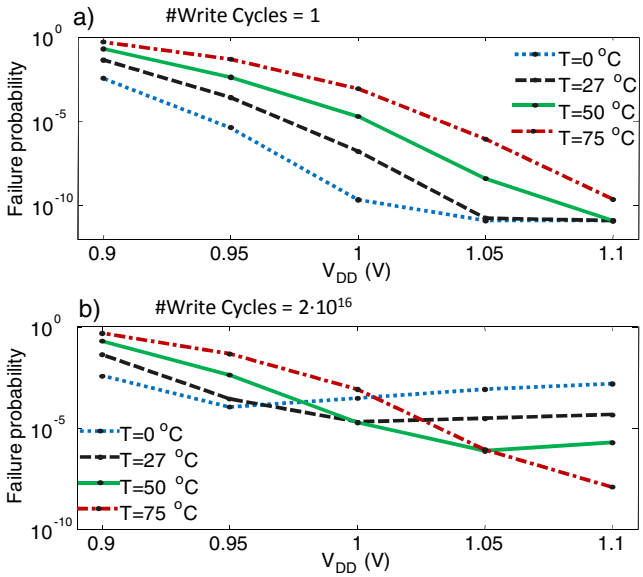

Fig. 5. STT-RAM cell failure probability as function of supply voltage at different temperatures under fabrication- and aging-induced process variability for a) "fresh" cell; b) aged cell

When evaluating the cell failure probability after $2 \cdot 10^{16}$ write operations we observe different trends than the ones observed for the fresh cell. In this situation, the failure probability degradation is no longer monotonic with the supply voltage increase over all temperatures (Fig. 5b). In all cases, except one (T=348K), after $2 \cdot 10^{16}$ write operations the cell failure probability is either in region 1) or 2) of the failure probability curve, depending on the temperature of operation. It should be noted that the reliability curves have a minimum. This is due to the fact the increasing the supply voltage has competing effects on the cell reliability. It improves the quality of both read and write operations, in this way decreasing the failure probability, but, on the other hand, it puts more stress on the tunneling oxide, in this way speeding the aging process and reducing the cell reliability.

All results obtained by device simulation and previously described and explained, are summarized in Fig. 6. Here we show the complete family of failure probability curves obtained under the stated conditions of process, voltage and temperature variations (Fig. 6a). Failure probability surface curves for extracted at different moments in the life time of the memory cell show how the effect of the supply voltage variation and temperature changes under different aging scenarios.

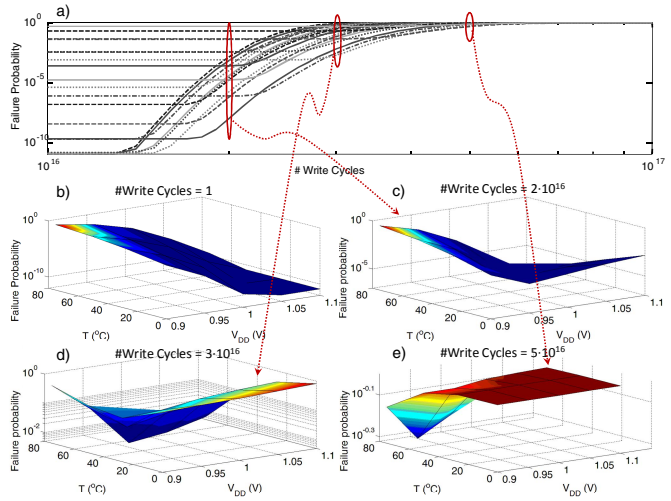

Fig. 6. STT-RAM cell failure probability under the joint effect of process, voltage and temperature (PVT) variations a) family of failure probability curves; cell failure probability levels for the b) fresh cell, c), d) and e) aged cell.

V. Conclusions

In this paper we describe a methodology for STT_MRAM cell reliability prediction under the joint effect of fabrication- and aging-induced process variability, supply voltage and temperature variations. Our results show that is paramount to understand and evaluate the voltage and temperature variation effect on the cell reliability all through at different instances in time to get a comprehensive and correct idea on how the cell actually behaves.

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