Power-Aware Voltage Tuning for STT-MRAM Reliability

## Memories Today

<table>
<thead>
<tr>
<th></th>
<th>SRAM</th>
<th>DRAM</th>
<th>Flash</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Cell Size</strong></td>
<td>120F²</td>
<td>4-6F²</td>
<td>4-5 F²</td>
</tr>
<tr>
<td><strong>Read Access Time</strong></td>
<td>&lt;1ns</td>
<td>20ns</td>
<td>25,000ns</td>
</tr>
<tr>
<td><strong>Write1 Access Time</strong></td>
<td>&lt;1ns</td>
<td>0ns</td>
<td>200,000ns</td>
</tr>
<tr>
<td><strong>Write0 Access Time</strong></td>
<td>&lt;1ns</td>
<td>20ns</td>
<td>200,000ns</td>
</tr>
<tr>
<td><strong>Endurance</strong></td>
<td>&gt;10³</td>
<td>10¹⁵</td>
<td>10⁴</td>
</tr>
<tr>
<td><strong>Non-volatility</strong></td>
<td>NO</td>
<td>NO</td>
<td>YES</td>
</tr>
</tbody>
</table>
Outline

• Introduction to STT-MRAM cell
• STT-MRAM cell operation principle
• STT-MRAM parametric reliability analysis
  – Failure mechanisms
  – Control voltage influence on memory cell operation
• STT-MRAM cell reliability estimation
• Conclusions
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The orientation of the free layer:
- determines the *resistance* of the material
- can be changed by injecting *current*.  

**MTJ – Magnetic Tunnel Junction**

- **Parallel State (P) ‘0’**
  - Low electrical resistance
- **Anti-parallel State (AP) ‘1’**
  - High electrical resistance
Main resiliency issues come from variations in:

- Tunneling oxide thickness and cross-section area
- Free layer thickness
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1T1MTJ STT-MRAM Cell

$I_{HL}$ – high to low transition
$I_{LH}$ – low to high transition
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STT-MRAM Failure Mechanisms

\( R_{\text{MTJ}} \) (a.u.)

\( V_{\text{DC}} \) (a.u.)

\( R_H \)

\( R_L \)

\( V_{\text{DC}} \) (a.u.)
STT-MRAM Failure Mechanisms

The diagram illustrates the failure mechanisms in STT-MRAM using a graph with axes $R_H$, $R_L$, $R_{HMAX-W}$, and $R_{LMAX-W}$. The area labeled "OK" represents the acceptable range, while the areas labeled "W0F" and "W1F" indicate regions where failure is more likely to occur. The graph also shows the relationship with $V_{DC}$ (a.u.).
STT-MRAM Failure Mechanisms

- $R_{HMIN}$
- $R_{LMAX}$
- OK
- $R_{1F}$
- $R_{0F}$
- TMRO

Graph showing $R_H$ versus $R_L$ with failure regions and boundaries.
STT-MRAM Failure Mechanisms
STT-MRAM Failure Mechanisms

\[ P_{RF \& WF} = 1 - \int_0^{\min(R_{LMAX-R}, R_{LMAX-W})} \int_{R_{HMIN-R}}^{R_{HMAX-W}} \int_{V_{TH-min}}^{V_{TH-max}} f(R_L, R_H, V_{TH}) dR_L dR_H dV_{TH} \]
Magnetic nanostructures suffer from thermally activated magnetization reversal.

Néel-Brown: at finite temperature, there is a finite probability for the magnetization to flip and reverse its direction.

Néel-Brown model:

\[ P(t) = \exp(t/\tau) \]
\[ \tau = \tau_0 \exp(\Delta E / k_B T) \]
STT-MRAM Failure Mechanisms

- STT-MRAM Cell Failure Probability in Data Retention:

\[ P(t) = 1 - \exp\left[\left(-\frac{Nt}{\tau_0}\right) \cdot \exp\left(-\frac{\Delta E}{k_B T}\right)\right] \]
STT-MRAM Failure Mechanisms

• STT-MRAM Cell Failure Probability in Read Operation

\[ P(t) = 1 - \exp\left[(-Nt/\tau_0) \cdot \exp(-\Delta E(1 - (I_{\text{read}}/I_{0C})/k_B T)) \right] \]
Aging: STT-MRAM Cell Failure due to Tunneling Oxide Breakdown

R_H degradation due to Tunneling Oxide stress:

\[ R_H(t) = \frac{R_H(0)}{1 + F(t)\left[\frac{R_H(0)}{R_H(t_{BD})} - 1\right]} \]

with F(t) following a Weibull distribution:

\[ F(t) = 1 - \exp\left(-\frac{t}{\lambda}\right)^k \]
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Control voltage effect on STT MRAM cell operation

Knobs

- $V_{DD}$
- $V_{WL}$
- $V_{BL-SL}$
Control voltage effect on STT MRAM cell operation

\[ P(t) = 1 - \exp\left(-\frac{Nt}{\tau_0}\right) \cdot \exp\left(-\frac{\Delta E}{k_B T}\right) \]

\[ P(t) = 1 - \exp\left(-\frac{Nt}{\tau_0}\right) \cdot \exp\left(-\frac{\Delta E(1 - (I_{\text{read}}/I_{\text{OC}}))}{k_B T}\right) \]
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STT-MRAM cell reliability

No knobs, Fresh Cell, 2D analysis with swipe $V_{TH}$
STT-MRAM cell reliability

No knobs, Aged Cell, 3D analysis

\[ 1 - P_{RF&WF}(t) \]

\( \# \text{ Write Pulses} \)
STT-MRAM cell reliability

$V_{DD}$ knob, Fresh Cell, 2D analysis with swipe $V_{TH}$

$P_{RF&WF}(0)$

$\Delta V_{TH} = 0.05V$

$\Delta V_{TH} = 0.03V$

$\Delta V_{TH} = 0V$

$\Delta V_{TH} = -0.03V$

$\Delta V_{TH} = -0.05V$
STT-MRAM cell reliability

V_{DD} knob, Aged Cell, 3D analysis

\( P_{RF\&WF}(t) \)

\[ \begin{align*}
\Delta V_{DD} / V_{DD-nom} (V) \\
-0.2 & -0.1 & 0 & 0.1 & 0.2 \\
10^{-12} & 10^{-10} & 10^{-8} & 10^{-6} & 10^{-4} & 10^{-2} & 10^0 \\
\end{align*} \]
STT-MRAM cell reliability

All knobs, Fresh Cell, 3D analysis

$P_{RF\&WF}(0)$ vs. $\Delta V/V_{\text{nom}}$ (V)

- $V_{WL}$
- $V_{DD}$
- $V_{BL-SL}$
- $V_{BB}$
STT-MRAM cell reliability

All knobs, Fresh Cell, 3D analysis

$t = 10^6$ cyc

$P_{RF\&WF}(t)$

$\Delta V/V_{nom}$ (V)

$V_{WL}$

$V_{DD}$

$V_{BL-SL}$

$V_{BB}$
**STT-MRAM cell reliability**

All knobs, 3D analysis

![Graph showing reliability](image)

- $V_{WL}$
- $V_{DD}$
- $V_{BL-SL}$
- $V_{BB}$

$t = 0\text{cyc}$ vs $t = 10^6\text{cyc}$
STT-MRAM cell reliability

All knobs, 3D analysis

$t = 0\text{cyc}$

$t = 10^6 \text{cyc}$

- $V_{WL}$
- $V_{DD}$
- $V_{BL-SL}$
- $V_{BB}$
Reliability Power Tradeoff

Power Consumption when varying $V_{WL}$

Power Consumption when varying $V_{DD}$

Failure Probability due to Read Disturb (RD)

$P_{RF\&WF}(t)$

$\Delta V/V_{\text{nom}} (V)$

$V_{WL}@t=0$

$V_{DD}@t=0$

$V_{WL}@t=10^{16} \text{ cyc}$

$V_{DD}@t=10^{16} \text{ cyc}$
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• STT-MRAM reliability evaluation methodology
• The joint effect of
  – fabrication- and aging-induced process variability
• Reliability evaluation under voltage tuning
• Power aware reliability estimation to identify optimum voltage value for STT-MRAM operation
Power-Aware Voltage Tuning for STT-MRAM Reliability