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Scope of the document

The objective of this deliverable is to report on the strategy for creating and publishing a final press releases including a summary of the work done in three years of research and development.

1. Introduction

In the CLERECO project, WP7 covers dissemination, exploitation and public awareness of the project. Within this WP, Task 7.1 (*Dissemination of project results*) is devoted to implement all forms of direct dissemination activities such as website creation, publication activities, workshop organization, and press releases. In particular, it plans 2 press releases: one initial press release, at the beginning of the project to inform the public about the beginning of the research activities and another release at the end of the project. The purpose of writing and circulating a press release at the end of the project is to:

- announce the end of the research activities,
- spread information and create awareness about obtained results,
- trigger out curiosity and create new opportunities for exploitation of the generated foreground.

The project final press release was designed at the end of the project (M38). The draft was created by the Coordinator (Politecnico di Torino) with the support of Impact: Engineering and Technology edition (<https://impact.pub/>) and was circulated among selected partners for a final review. The text of the press release is reported in the following section while the final formatted file is available in Appendix I. The collaboration with a professional publisher for the creation of the content allowed for the creation of a high quality text and graphical look required at the end of the project to attract potential stakeholders. Moreover, the publisher granted the access to a wide network of contacts, thus improving our capability to reach a wider audience.

2. Press release raw text

Header: Design for reliability in the era of the computing continuum

Standfirst: The CLERECO collaborative project proposes a scalable, cross-layer methodology and supporting suite of tools for accurate and fast estimations of computing systems' reliability using an innovative component-based Bayesian model that holistically accounts for the effect of the technology, the hardware architecture and the software executed in the system. ///

Body text

As we enter the era of nanoscale devices, reliability is becoming a key challenge for the semiconductor industry. The now atomic dimensions of transistors result in a vulnerability to variations in the manufacturing process and can rise dramatically the effect of environments stress on the correct circuit behavior. Failures in early assessing computing systems' reliability may produce excessive redesign costs which can have severe consequences for the success of a product.

Current practice involves a worst-case design approach with large guard bands. Unfortunately, application of this approach is reaching its limit in terms of economic sustainability with regard to performance, size and energy costs. Coordinated by Dr Stefano Di Carlo of the Politecnico di Torino in Italy, the CLERECO (Cross Layer Early Reliability Evaluation for the Computing cOntinuum) project aims to address this challenge.

The CLERECO project involves industrial and academic partnerships between four academic institutions and three manufacturers in order to create a new approach and new tools for electronic design automation (EDA) support in reliability assessment. The project addresses a key challenge faced by designers employing early measures to prevent hardware faults propagating to the software layers of the system stack and reaching the system output. Different protection mechanisms must be employed at each layer in order to provide 'cross-layer' reliability enhancement. This challenge becomes more serious when coupled with the concept of the 'computing continuum'. This phrase was coined by Intel already in 2011 and describes the erosion of the traditional separation between the market segments of embedded systems and high performance computing systems. CLERECO aims to reflect this merging of market segments at the EDA level by providing tools that can be applied with small differences to different computer architectures and across a range of areas. CLERECO has been in operation since 2013, with key milestones including theoretical models, tool design, adaptation of tools for industry use, and commercialization of the created tools by partner organizations.

Subhead: A new methodology and approach

The CLERECO project focuses on reliability analysis in the early phases of the design. Early assessment within the design cycle provides the freedom for adaptive modification if the estimated reliability level does not meet the requirements. Traditional tests typically take place at the end of the design stage when a prototype of the system is available. Physical stress tests are generally used to evaluate the final reliability of a system. When working with models of the design, register transfer level or gate level fault injection (FI) is the most accurate standard method for performing reliability analysis. The designer creates a detailed model of the system hardware and is able to simulate the execution of software applications on this model. To perform reliability analysis, faults are artificially injected into the model, thus simulating what could happen in a real environment, and the effect of the faults are evaluated by comparing the behavior of the faulty system with a fault-free version. Theoretically, by performing a statistically significant number of simulations a very precise estimation of the reliability of the system can be identified.

Di Carlo identifies problems with this approach: 'These detailed gate-level models, especially for complex hardware blocks such as microprocessors are not always available, and the simulation time in case of complex systems is prohibitive. Usually this results in the use of simplified simulations and models.' This leads, in Di Carlo's opinion, to 'inaccurate and usually pessimistic estimations'.

CLERECO methodology addresses this challenge by providing dedicated tools to separately analyze the technology, the hardware components (at the microarchitecture level) and the software modules of a complex system and to recombine the characteristics of single object into a complex statistical Bayesian model that can be used to perform statistical reasoning on the reliability of the system as a whole. As part of the project a comparative analysis between reliability estimations obtained using CLERECO models and tools on a set of benchmark and real systems and results obtained using an accurate gate level FI campaign and a simplified FI approach both performed using state-of-the-art commercial tools has taken place. The results revealed an equivalent level of estimated reliability, with a significant reduction in simulation time required when using a CLERECO reliability estimation approach versus an industry standard gate level FI campaign.

Subhead: Industrial challenges

Di Carlo describes several challenges faced during the project in relation to the stability of the industrial team: 'Within three years there were three changes in the composition of the industrial consortium. Intel Corporation Iberia S.A. (Spain) left the consortium after eight months due to closure of the local facility; similarly, after 18 months ABB AS (Norway) left due to closure of the local facility and ABB activities moved to ABB AB (Sweden); and finally Yogitech SpA was acquired by Intel at the end of the project, producing another change and bringing Intel Corporation Italia SpA in the consortium.'

The project remained intact but the turbulence created by such changes represented a significant overhead for Di Carlo and in some cases represented a threat to the continuation of the project. The ability to weather such turbulence relied on the preventive definition of effective backup plans for these situations and on the research strength and dedication of the all-academic partners that guaranteed the smooth continuation and the successful completion of the project.

This instability of the industrial consortium is not unique to the CLERECO project, however. The current situation within the global economy as well as the speed at which IT business changes make a three- year commitment in a research project increasingly difficult for industrial partners. In contrast to this, Di Carlo explains, 'There were few major scientific challenges and there was a good and very productive collaboration among all partners.'

Subhead: Market-ready results

Industrial partners have been very important during the project despite the changes mentioned above. CLERECO worked in collaboration to build tools that could be inserted directly into industrial design flows. As Di Carlo outlines, 'There are so many academic tools around that don't find real application in the industry since they are not built to be integrated into a real industrial design flow.' Industrial partners, provided guidelines on the use of tools and models, thus creating a key area of value for the project. Di Carlo notes that the 'complexity of the new technologies requires a deeper collaboration between industry and academia. We could not have achieved our results without the strong support of our industrial partners'.

Industrial partners also provided systems on which the tools and models were tested. Benchmarks are effective instruments for evaluation of the capability of a tool but only when working with real cases can the practical limits of an approach be understood. This academic and industrial partnership allowed a move from laboratory-based benchmark analysis to real systems in order to identify system-based bottlenecks. These have now been corrected, allowing delivery of mature products.

Industrial partners also provided the tools and knowledge to perform a fair comparison of CLERECO methods with existing gold standard commercial products. In particular, Yogitech SpA had already commercialized products for reliability analysis based on gate level FI. Due to the contribution of Yogitech it was possible to compare the CLERECO early reliability estimation tools with a commercial reliability analysis workflow, showing how early reliability analysis can complement precise FI based validation at the end of the design flow. CLERECO partners also provide a channel for exploitation and presentation of the project's results. The CLERECO team has presented at HiPEAC Conference, DATE (Design Automation and Test in Europe), ISPASS (International Symposium on Performance Analysis of Systems and Software), VTS (IEEE VLSI Test Symposium), ICCD (IEEE International Conference on Computer Design), IOLTS (IEEE International Symposium on On-Line Testing and Robust System Design), PATMOS (International Workshop on Power And Timing Modeling, Optimization and Simulation), DCIS (Design of Circuits and Integrated Systems Conference) and CTC (China Test Conference) in 2016 alone, and have an upcoming presentation of their exciting results at the ITC (IEEE International Test Conference) in Dallas in November 2016.

Pull Quote: 'The complexity of the new technologies requires a deeper collaboration between industry and academia. We could not have achieved our results without the strong support of our industrial partners'

3. Media coverage

The press release has been distributed to the following agencies/media:

Impact: Engineering and Technology edition <https://impact.pub/>

Impact is a quarterly publication designed to provide an open access platform for researchers to communicate the aims, objectives and potential socioeconomic and academic impact of their research. The aim of the open access publication is to provide a platform for researchers to impact a broader scientific and societal audience, by having their research communicated in a clear and transparent format. The Impact publication is promoted to 35,000 individuals worldwide within academia, government, research centers, funding agencies and research councils. The CLERECO press release will be online in the February 2017 issue.

IngentaConnect - www.ingentaconnect.com

One of the world's largest resource for scholarly publications. There are over 24,000 librarians in Europe and 21,000 in the USA, from both the public and private sector, whom are registered to access content from this resource. The CLERECO press release is freely available on IngentaConnect and as a result of this, shall be available through Google Scholar, EBSCO, Primo Central and World Cat Discovery, while also receiving a Crossref DOI and be deposited in Portico repositories.

EDACafè - http://www10.edacafe.com/nbc/articles/view_article.php?articleid=1474273

The EDACafè target audience is IC, FPGA, Printed Circuit Board, and System designers and managers. EDACafè reaches out to companies who are the end users of these tools and the decision makers who purchase them. The CLERECO press-release has been submitted for publication on the EDACafè website. Moreover, EDACafè distributed the press-release to more than 30,000 professionals as part of the EDACafe.com daily newsletter.

HiPEAC

HiPEAC is the European Network of Excellence (NoE) on High Performance and Embedded Architecture and Compilation. The CLERECO press release has been submitted to the HiPEAC communication contact in order to be announced through the HiPEAC website, the HiPEAC

newsletter and the HiPEAC magazine, the three communication channels offered by the network.

CLERECO website, list and CLERECO partners' websites

The press release has been posted on the CLERECO website and also posted on the partners' local websites.

Appendix 1: CLERECO Press release

Impact Objectives

- Develop early and accurate evaluations of the reliability of an electronic system
- Support the development of scaled electronic systems

Rethinking reliability evaluation within electronic systems

Dr Stefano Di Carlo of the Department of Control and Computer Engineering at the Polytechnic University of Turin is Coordinator of the CLERECO project, and below he discusses the importance of accurate reliability evaluation within the emerging computing continuum



First, can you briefly outline the overall focus of the CLERECO project?

CLERECO (Cross Layer Early Reliability

Evaluation for the Computing cOntinuum) is an electronic design automation (EDA) project. Instead of delivering a product such as a computer, an operating system or application software, we produce software tools to be used by the designers of complex electronic systems. The project focuses on the digital portion of a complex system and thus analogue devices are outside the scope of our project.

Can you explain what Bayesian networks are and describe their novel use within your research?

Bayesian networks are a well-known statistical model for performing statistical reasoning on the causes and effects of stochastic events. When discussing system reliability in relation to hardware faults, Markov models have traditionally been used. Prior to this project, Bayesian models have largely been used in the software reliability field. Software reliability is also an important factor, but it differs from reliability in relation to hardware faults. Software reliability reflects the software design perfection, while in CLERECO we focus on modelling the system behaviour in the presence of faults. In this sense our usage of Bayesian networks is quite novel. In addition to applying the concept within a new area the team has also improved traditional Bayesian networks with

new concepts. These concepts are devoted to specifically modelling the different layers composing a complex digital system that include the technology, the hardware architecture and the executed software.

The Bayesian model is a key element of the work done. However, this model is multifarious and cannot be constructed extemporaneously. Without the availability of dedicated tools, the idea of the Bayesian model for a traditional designer would remain a theoretical exercise. Within CLERECO a great deal of work has taken place to design such tools which bridge the gap between theory and practice. Microarchitectural models of the hardware architecture and virtualised software models are two of the main examples of the concepts we integrated in our tools to support the development of our Bayesian model.

What are the consequences of false negatives or false positives in the CLERECO method and do they present a risk?

There is a clear difference in occurrence rates between the two, however the CLERECO project aims to minimise both types. We define a false positive as a system whose reliability is underestimated since the actual probability of fault would be lower than its estimated value and conversely a false negative as a system whose reliability is overestimated. False positives ultimately do not risk the safety and stability of the system but result in over-design and so would waste resources in order to reach the desired reliability level. With a false negative the

underestimation of a problem could result in serious consequences for the operation and usability of the system. In comparing the risks of false positive and false negatives it is clear that false negatives need to be avoided and in our work we strive to follow this philosophy.

The key point is that the CLERECO tools are designed to provide rapid reliability estimation during the initial part of the design stage to aid decision-making. The tools do not substitute all tests required for a prototyped system when assessing its final reliability. Accordingly, in both cases the risks would impact the need to redesign the system due to the fact that the final reliability level is different from the one estimated in the early phases.

Why is CLERECO important at the design stage?

Our tools help designers understand how a technology, hardware architecture and application software work together in a complex system. This results in an understanding of the system's reaction to sources of failure which arise during work in the field. Advanced knowledge of the threats a system will encounter during its lifetime allows the designer to appropriately allocate the countermeasures implemented and ensure these threats will not impact upon the safety of the users. This challenge of implementing fault tolerance is a key area of cost in terms of system performance, energy consumption, component size and design time.

Design for reliability in the era of the computing continuum

I The CLERECO collaborative project proposes a scalable, cross-layer methodology and supporting suite of tools for accurate and fast estimations of computing systems' reliability

As we enter the era of nanoscale devices, reliability is becoming a key challenge for the semiconductor industry. The now atomic dimensions of transistors result in a vulnerability to variations in the manufacturing process and can dramatically increase the effect of environmental stress on the correct circuit behaviour. Failures in early assessing computing systems' reliability may produce excessive redesign costs which can have severe consequences for the success of a product.

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A NEW METHODOLOGY AND APPROACH

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systems is prohibitive. Usually this results in the use of simplified simulations and models.' This leads, in Di Carlo's opinion, to 'inaccurate and usually pessimistic estimations'. CLERECO methodology addresses this challenge by providing dedicated tools to separately analyse the technology, the hardware components (at the microarchitecture level) and the software modules of a complex system and to recombine the characteristics of single objects into a complex statistical Bayesian model. This can be used to perform statistical reasoning on the reliability of the system as a whole.

As part of the project a comparative analysis was undertaken to compare reliability estimations gathered using the CLERECO tools with those obtained using an accurate and a simplified gate-level fault injection campaign. The results revealed an equivalent level of estimated reliability, with a significant reduction in simulation time required when using a CLERECO reliability estimation approach versus an industry standard gate-level FI campaign.

INDUSTRIAL CHALLENGES

Di Carlo describes several challenges faced during the project in relation to the stability of the industrial team: 'Within three years there were three changes in the composition of the industrial consortium. Intel Corporation Iberia SA (Spain) left the consortium after eight months due to closure of the local facility; similarly, after 18 months ABB AS (Norway) left due to closure of the local facility and ABB activities moved to ABB AB (Sweden). Finally, Yogitech SpA was acquired by Intel at the end of the project, producing another change and bringing Intel Corporation Italia SpA in the consortium.'

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“The complexity of the new technologies requires a deeper collaboration between industry and academia. We could not have achieved our results without the strong support of our industrial partners”

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MARKET-READY RESULTS

Industrial partners have been very important during the project despite the changes mentioned above. CLERECO worked in collaboration to build tools that could be inserted directly into industrial design flows. As Di Carlo outlines, ‘There are so many academic tools around that don’t find real application in the industry since they are not built to be integrated into a real industrial design flow.’ Industrial partners, provided guidelines on the use of tools and models, thus creating a key area of value for the project. Di Carlo notes that the ‘complexity of the new technologies requires a deeper collaboration between industry and academia. We could not have achieved our results without the strong support of our industrial partners’.

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partnership allowed a move from laboratory-based benchmark analysis to real systems in order to identify system-based bottlenecks. These have now been corrected, allowing delivery of mature products.

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SHARING KNOWLEDGE

CLERECO partners also provide a channel for exploitation and presentation of the project’s results. In 2016 alone the CLERECO team has presented at the Institute of Electrical and Electronics (IEEE) Engineers ITC (International Test Conference) in Dallas, HiPEAC Conference, DATE (Design Automation and Test in Europe), ISPASS (International Symposium on Performance Analysis of Systems and Software), VTS (IEEE VLSI Test Symposium), ICCD (IEEE International Conference on Computer Design), IOLTS (IEEE International Symposium on On-Line Testing and Robust System Design), PATMOS (International Workshop on Power And Timing Modeling, Optimization and Simulation), DCIS (Design of Circuits and Integrated Systems Conference) and CTC (China Test Conference).

Project Insights

FUNDING

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PARTNERS

Polytechnic University of Turin (Stefano Di Carlo) • National and Kapodistrian University of Athens (Professor Dimitris Gizopoulos) • French National Center for Scientific Research (CNRS) (Dr Giorgio Di Natale and Professor Alberto Bosio) • Polytechnic University of Catalonia (UPC) (Professor Antonio González and Dr Ramon Canal) • Thales SA (Dr Arnaud Grasset) • Intel Corporation Italia SpA (formerly Yogitech SpA) (Dr Riccardo Mariani) • ABB AB (Dr Tiberiu Seceleanu)

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Dr Stefano Di Carlo has been an Associate Professor in the Department of Control and Computer Engineering at the Polytechnic University of Turin since 2014. He holds a PhD (2003) and an MS equivalent (1999) in Computer Engineering and Information Technology from the same institution. Di Carlo’s research areas include reliability analysis, field-programmable gate array design, memory testing, reliability analysis of non-volatile memories with error correction coding, design for testability, built-in self-test, fault simulation and automatic test generation. He is author of more than 100 scientific publications in international peer-reviewed journals and 1 patent application.

