Clereco

Cross-Layer Early Reliability Evaluation for the Computing cOntinuum

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http://www.clereco.eu

CLERECO project overview

Hipeac CSW at Barcelona

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PROJECT GOAL

CLERECO is a FP7 ICT collaboration project aiming at defining a new framework for Cross-Layer Early Reliability Evaluation for the Computing cOntinuum

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OUTLINE

- Motivation
- Overview of the activities
- Conclusions

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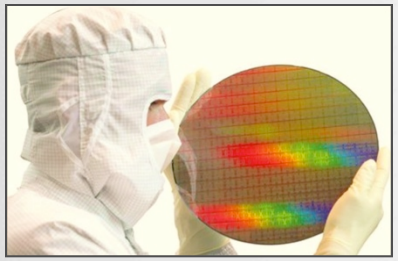
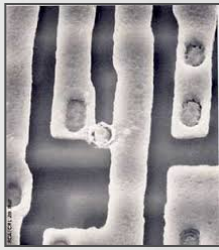
MOTIVATION



Aggressive shrinking of devices (<10nm)



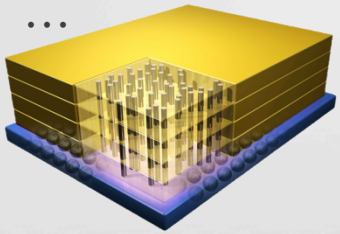
Increased aging an process variability

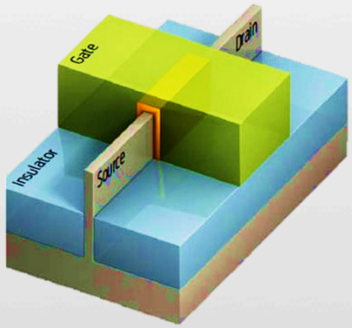
Increased susceptibility to the environment

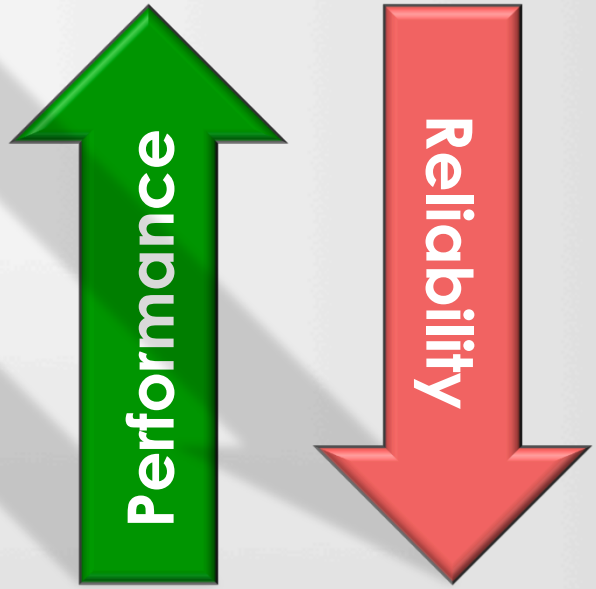
- Temperature
- Humidity
- Radiations
- …

New technological processes:

- FinFET
- Scaled bulk
- 3D integration
- Spin logic
- …







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MOTIVATION

Same key technologies and industrial players will act across all computing segments

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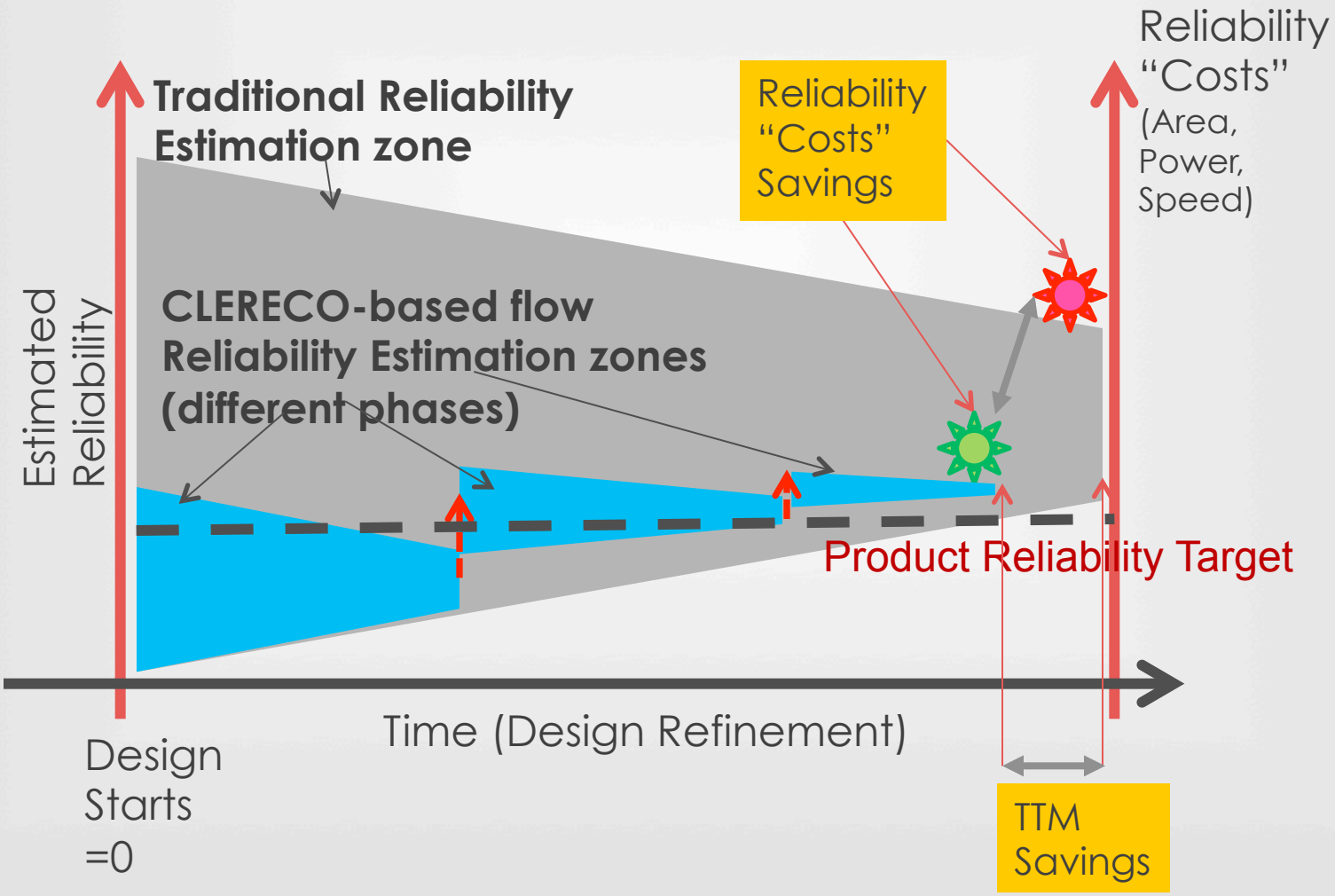
MOTIVATION



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CONSORTIUM

POLITECNICO DI TORINO 1859 1906

Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier
LIRMM

intel

THALES

YOGITECH

ABB

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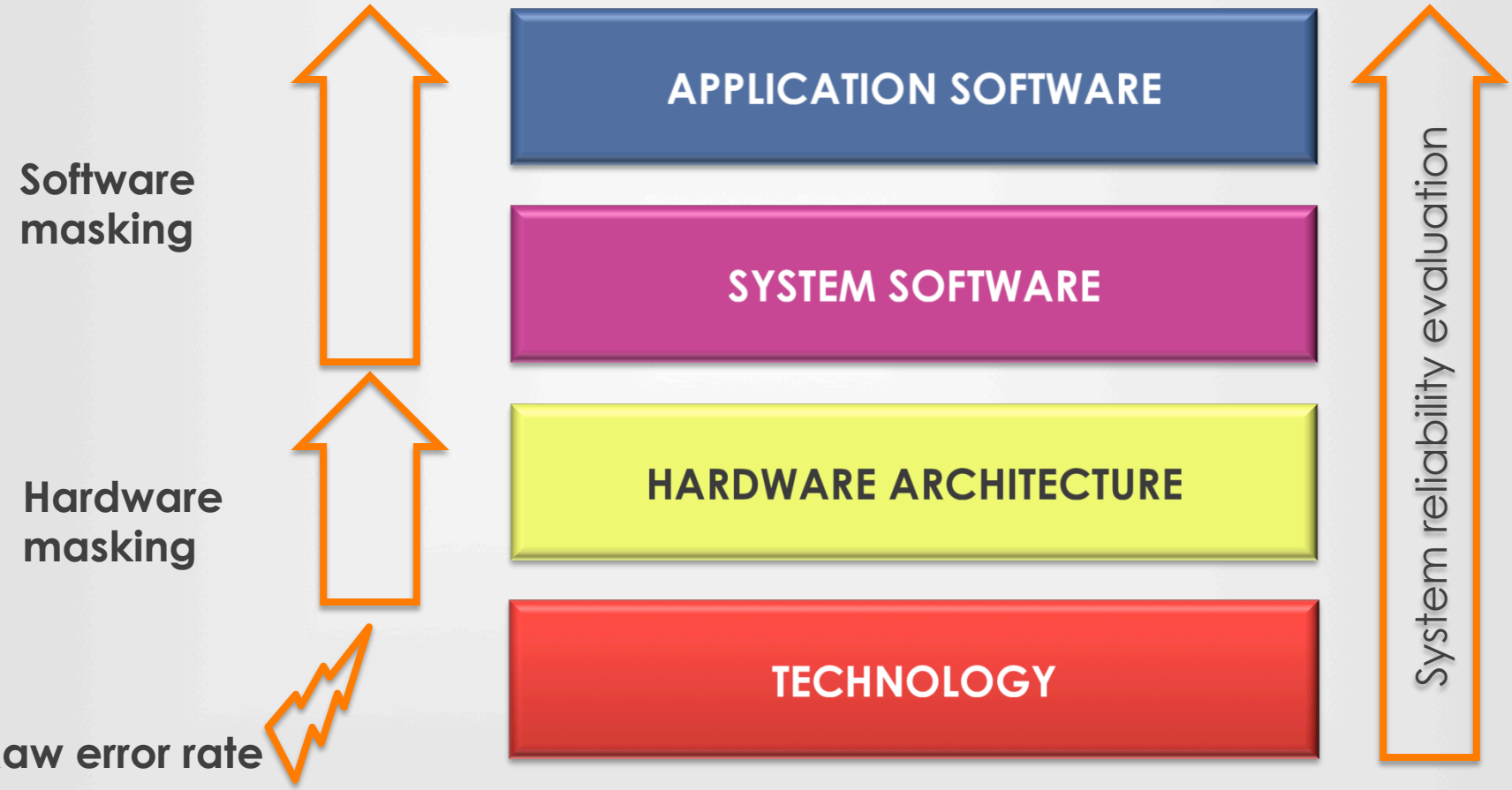
OVERVIEW OF THE ACTIVITIES



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CLERECO: the general vision

- Impact of hardware faults on:
  - Functionality
  - Performance
  - Power

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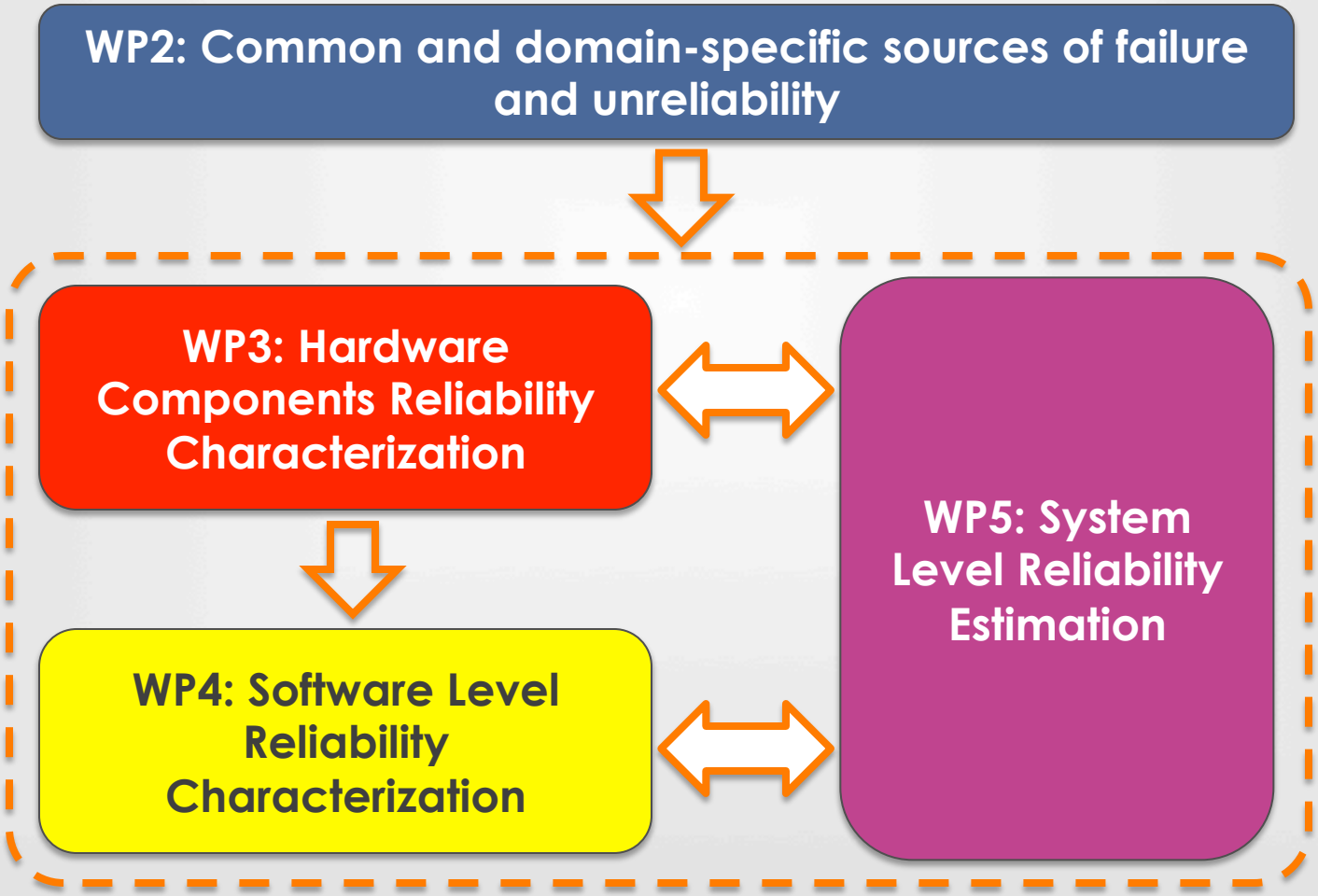

WP2: Common and domain-specific sources of failure and unreliability

- Analysis of the different failure mechanisms that will be relevant for the computing continuum (scaled bulk CMOS, III-V Ge, Finfets, spin logic, etc.)
- Identification and characterization of the main sources of failure
- Reliability requirements for the different computing segments within the computing continuum such as ES and HPC.
- Definition of the different operating modes of the system (e.g., voltage and frequency levels), and the different operating conditions (e.g., temperature, electronic noise, etc.) that may affect reliability

WP3: Hardware components reliability characterization

- Hardware systems are iteratively broken down into their basic components and characterized form the reliability standpoint
  - Computation of specific parameters and measures potentially impacting the overall system reliability
- Classes of considered components:
  - CPUs
  - Memories (e.g., DRAM, SRAM, Flash, RRAM, etc.)
  - Accelerators (e.g., GPUs)
  - Peripherals
  - Interconnects

WP4: SW level reliability characterization

- The software stack is break up into its basic components (from high-level application software modules down to the instruction set architecture level) and analyzes how hardware errors propagate through the software stack
- To allow early reliability estimation when the hardware architecture is still not defined WP4 aims at defining metrics and models enabling to abstract the behavior of the software from a specific hardware architecture

WP5: System level estimation models

- Measures and analyses performed in WP3 and WP4 are integrated into a comprehensive statistical framework able to estimate reliability metrics defined in WP2 (iteratively in the different design stages of the system)
- Estimated reliability metrics are used to develop algorithms able to support the designers in the reliability related decision-making process that will in turn allow the design of reliable systems with improved cost-related characteristics (area, energy/power, and performance) and reduced TTM

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Conclusions

- The characteristics that CLERECO pursues for its framework are:
  - **Flexibility**: reliability analysis must be possible starting from the very early design stages
  - **Speed**: time-consuming simulations and/or fault-injection campaigns must be avoided and replaced by accurate statistical models and procedures
  - **Accuracy**: reliability estimations must be as precise as possible.
  - **Comprehensiveness**: a heterogeneous set of target systems must be analyzable ranging from very application-dependent ES to more general-purpose HPC systems

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THANK YOU FOR YOU ATTENTION!