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Cross-Layer Early Reliability Evaluation for the Computing cOntinuum

Stefano Di Carlo, Alessandro Vallero (PoliTo)
Dimitris Gizopoulos (UoA)
Giorgio Di Natale (LIRMM)
Arnaud Grasset (Thales)
Riccardo Mariani (Yogitech)
Frank Reichenbach (ABB)

Cross-Layer Early Reliability Evaluation for the Computing cOntinuum (CLERECO)

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cal@di

University of Athens
Computer Architecture Lab

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CLERECO PROJECT GOAL

CLERECO is an FP7 ICT collaboration project aiming at defining a new framework for Cross-Layer Early Reliability Evaluation for the Computing cOntinuum

Reliability Evaluation

Early + Cross-Layer + Computing cOntinuum

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OUTLINE

- Motivation and Research Problem
- Overview of the project activities
- Conclusions

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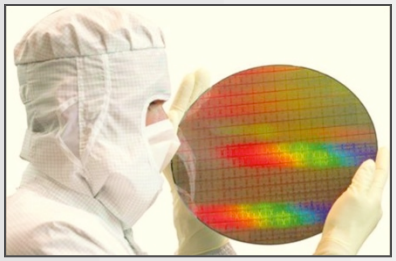
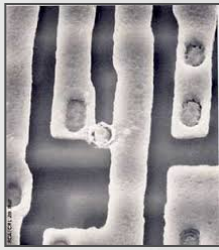
MOTIVATION



Aggressive shrinking of devices (<10nm)

Increased aging and process variability

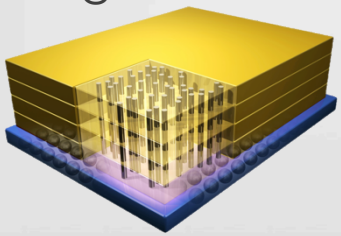


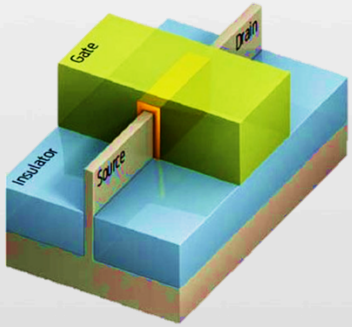
Increased susceptibility to environmental factors

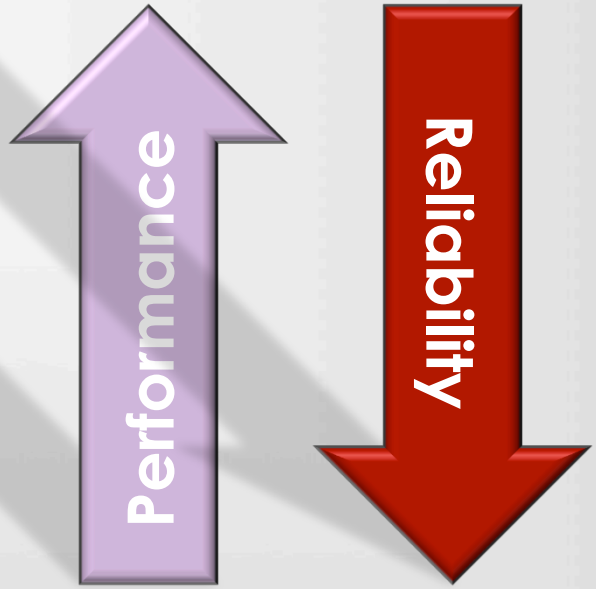
- Temperature
- Humidity
- Radiations
- …

New technological processes:

- FinFET
- Scaled bulk
- 3D integration
- Spin logic
- …







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RESEARCH PROBLEM

- Evaluate the **Reliability*** that a Computing System is expected to have during its operational lifetime with respect to **transient** + **intermittent** + **permanent** hardware faults due to the previous factors.

* **FIT** (Failures In Time), **MTBF** (Mean Time Between Failures), **or other metrics**

Reliability Evaluation

Early + Cross-Layer + Computing cOntinuum

EARLY RELIABILITY EVALUATION

- **How Early ?**
  - As early as possible in the design of the system
    - Specs
    - Architecture
    - Many Hardware and Software components still not known
- **Why evaluate reliability early ?**
  - Decide best protection mechanisms early
    - To save (re-)design costs
    - To save hardware and software costs (avoid over-design)
    - To save power/energy

CROSS-LAYER RELIABILITY EVALUATION

- **All system layers: hardware + software**
  - The **full system reliability** matters
  - Single-layer protection mechanisms **are not sufficient**
    - Hardware-based protection usually too expensive
      - e.g. low-level detection/correction schemes may correct errors that won't affect the application
    - Software-based protection usually less accurate
      - e.g. high-level sw-based detection schemes may miss errors
- **In forthcoming computing systems**
  - Errors due to hardware faults will happen **frequently**
  - **Cross-layer protection** schemes (detection + diagnosis + recovery + repair) will be needed

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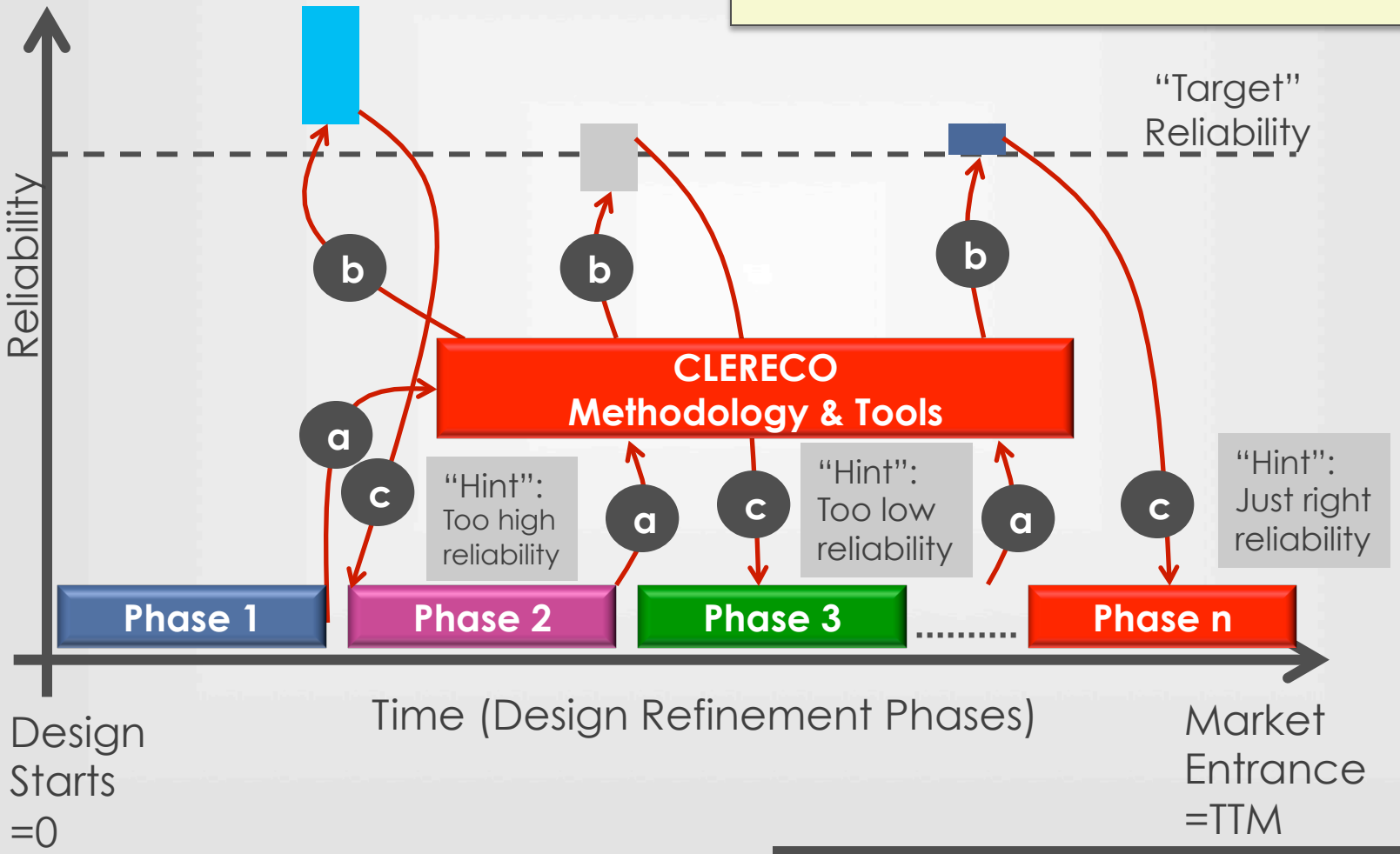
CLERECO-BASED SYSTEM DESIGN

a = HW & SW "known" Information Passed to CLERECO Framework from Phase k (1…n)

b = CLERECO Framework Reliability Estimation for Phase k

c = CLERECO "Hints" to Design Team for Phase k + 1



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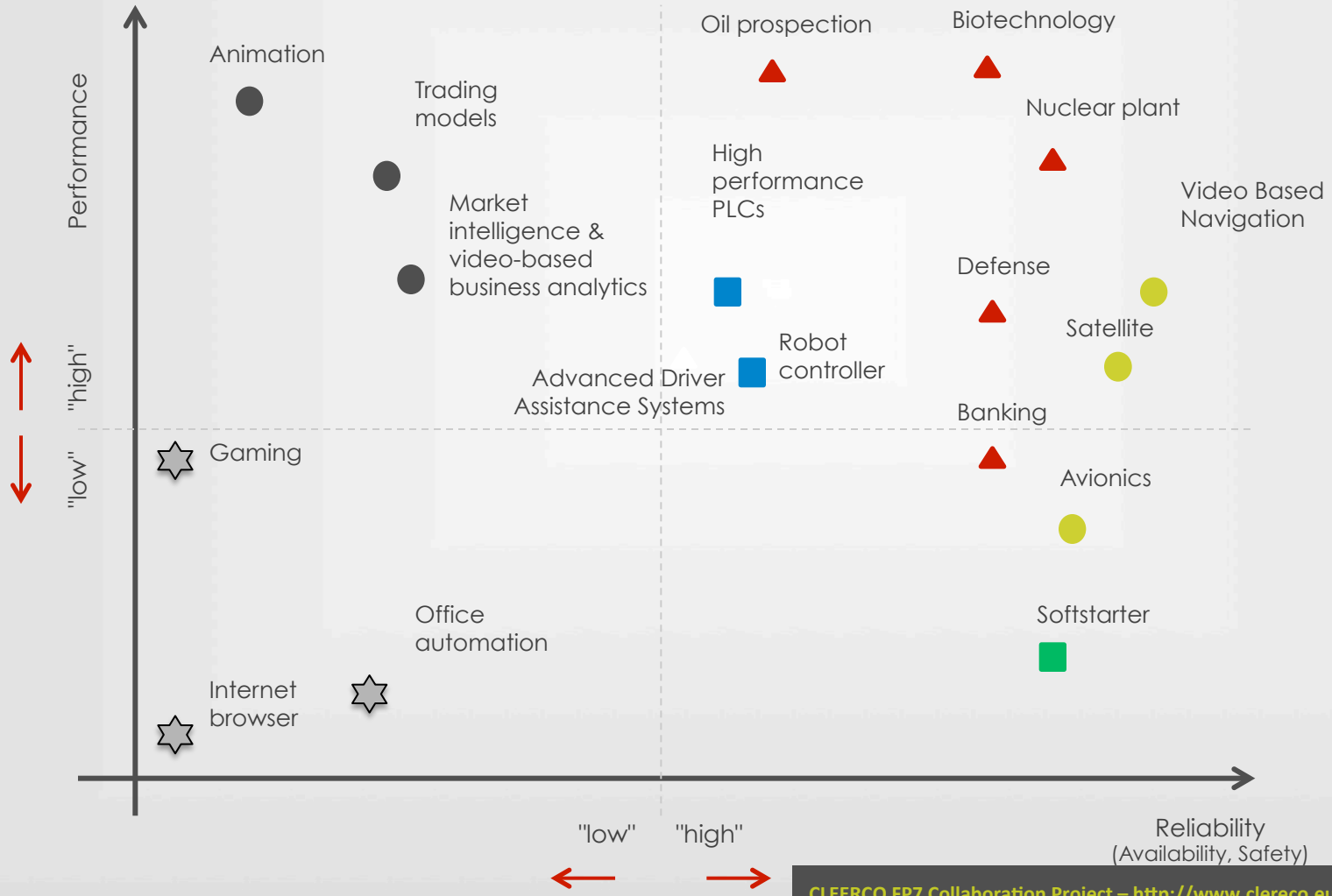
RELIABILITY IN THE COMPUTING CONTINUUM

Same key technologies and industrial players will act across all computing segments

APPLICATION DOMAINS IN THE COMPUTING CONTINUUM



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CLERECO MAIN OBJECTIVE

- **Save Reliability-related costs** by **Early and Accurate Estimation of the Full-system Reliability**

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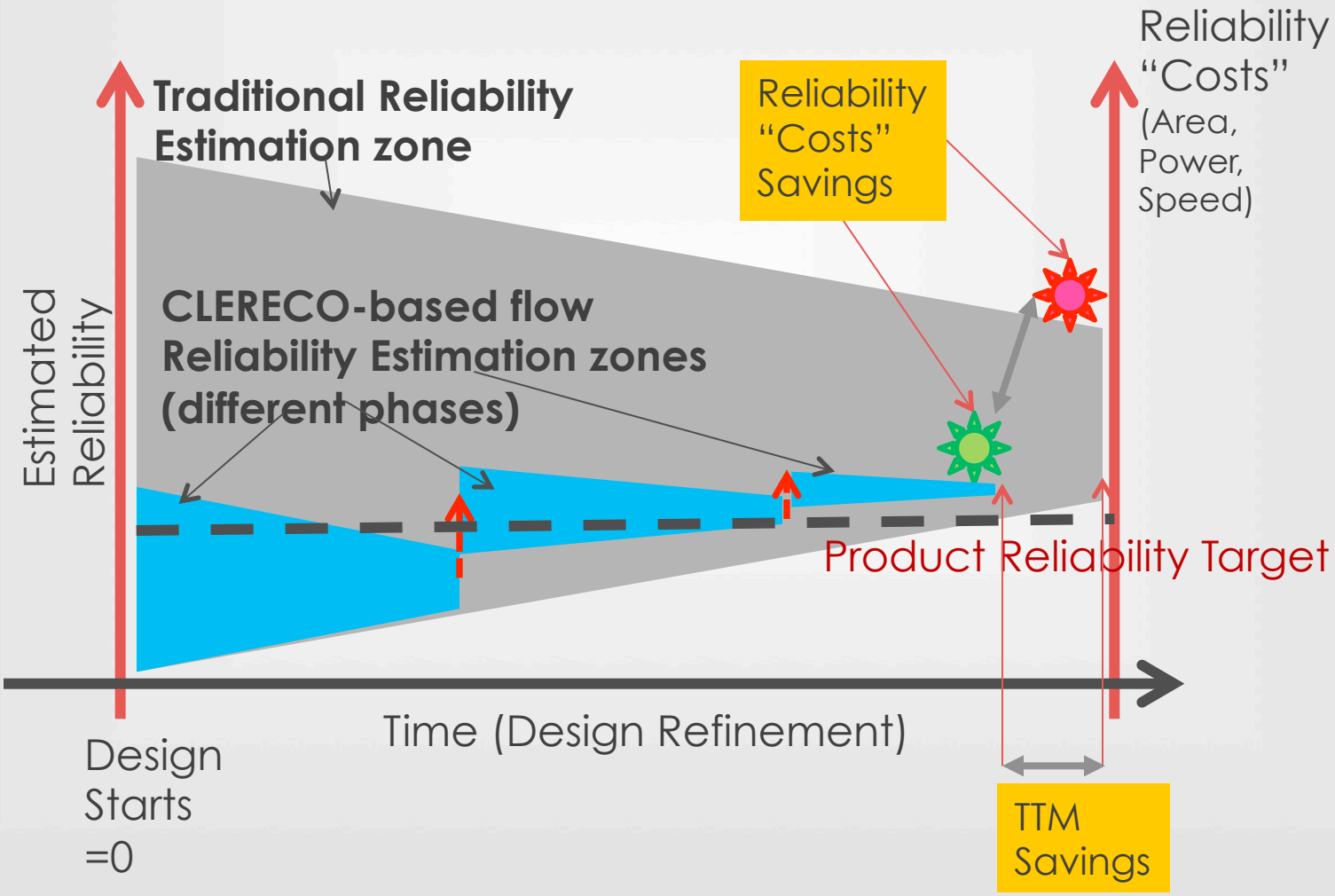
CLERECO MAIN OBJECTIVE VISUALIZED



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CLERECO CONSORTIUM

POLITECNICO DI TORINO 1859 1906

Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier
LIRMM

intel

THALES

YOGITECH

ABB

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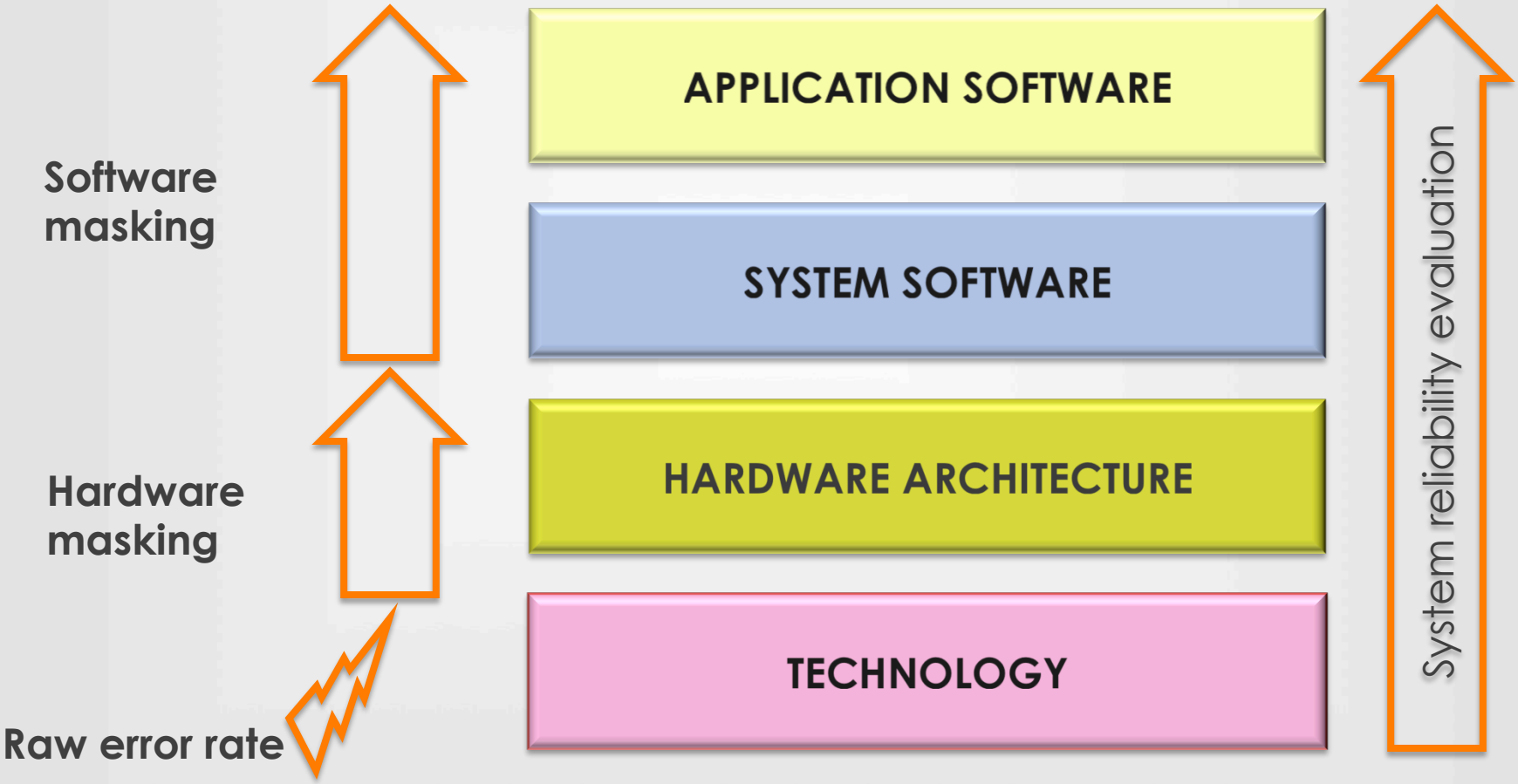
OVERVIEW OF THE TECHNICAL ACTIVITIES



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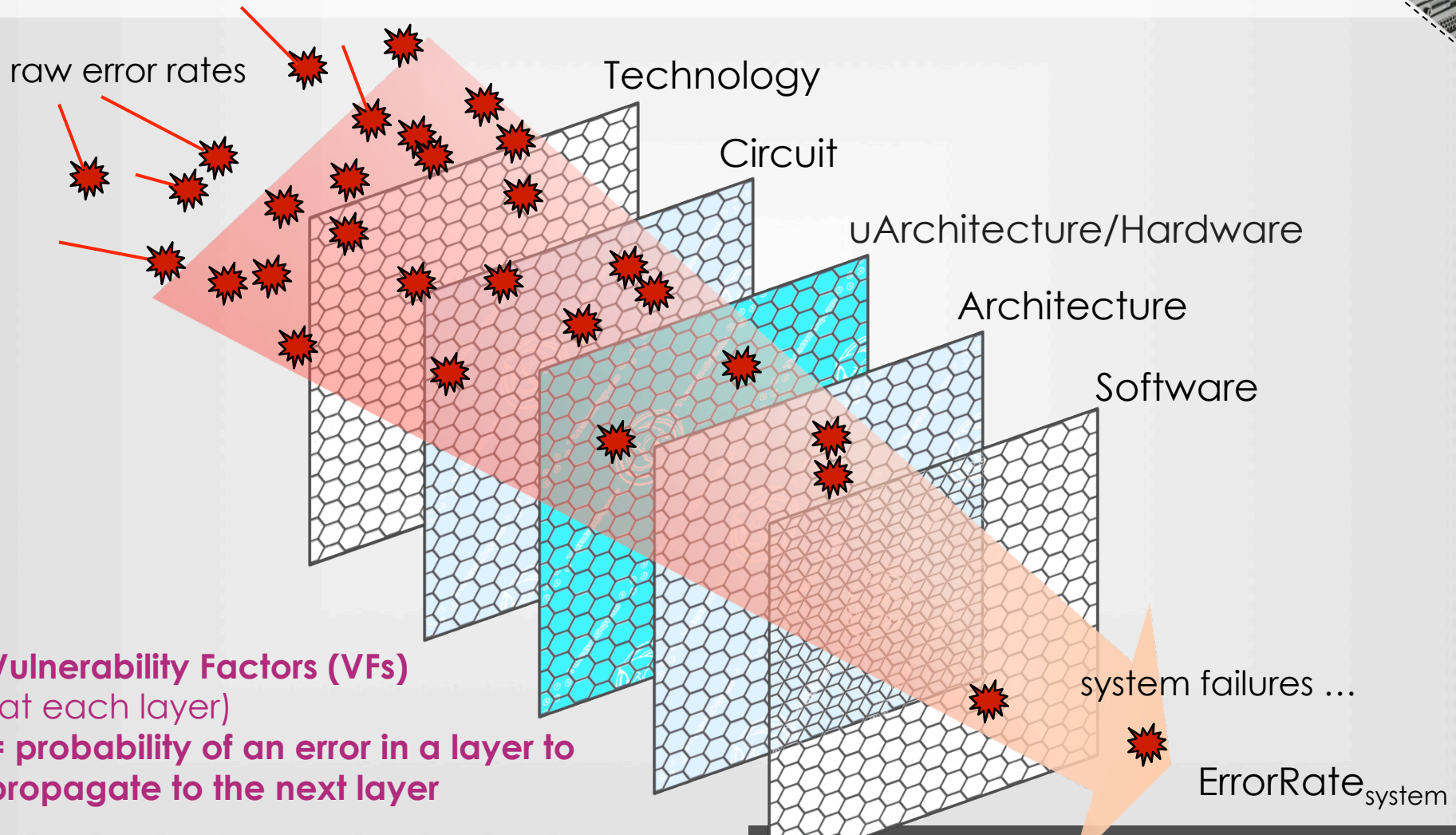
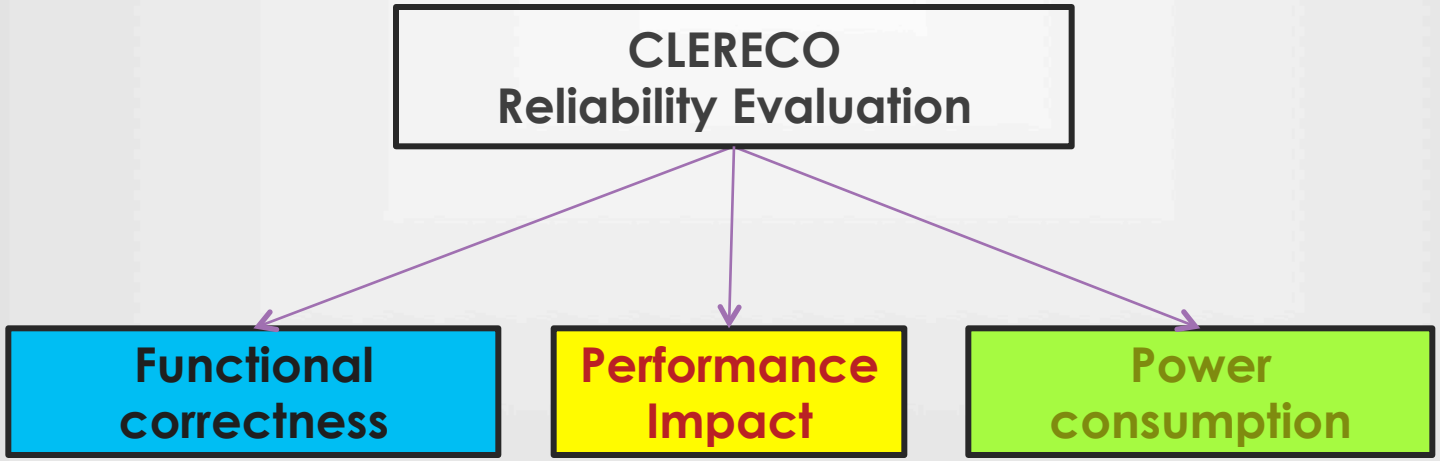
FULL-SYSTEM RELIABILITY IMPACT OF HARDWARE FAULTS



Vulnerability Factors (VFs)
(at each layer)
= probability of an error in a layer to propagate to the next layer

ASPECTS OF RELIABILITY CONSIDERED

- CLERECO considers the impact of hardware faults on:
  - **Functionality (correctness)**
  - **Performance (latency/throughput)**
  - **Power/Energy**



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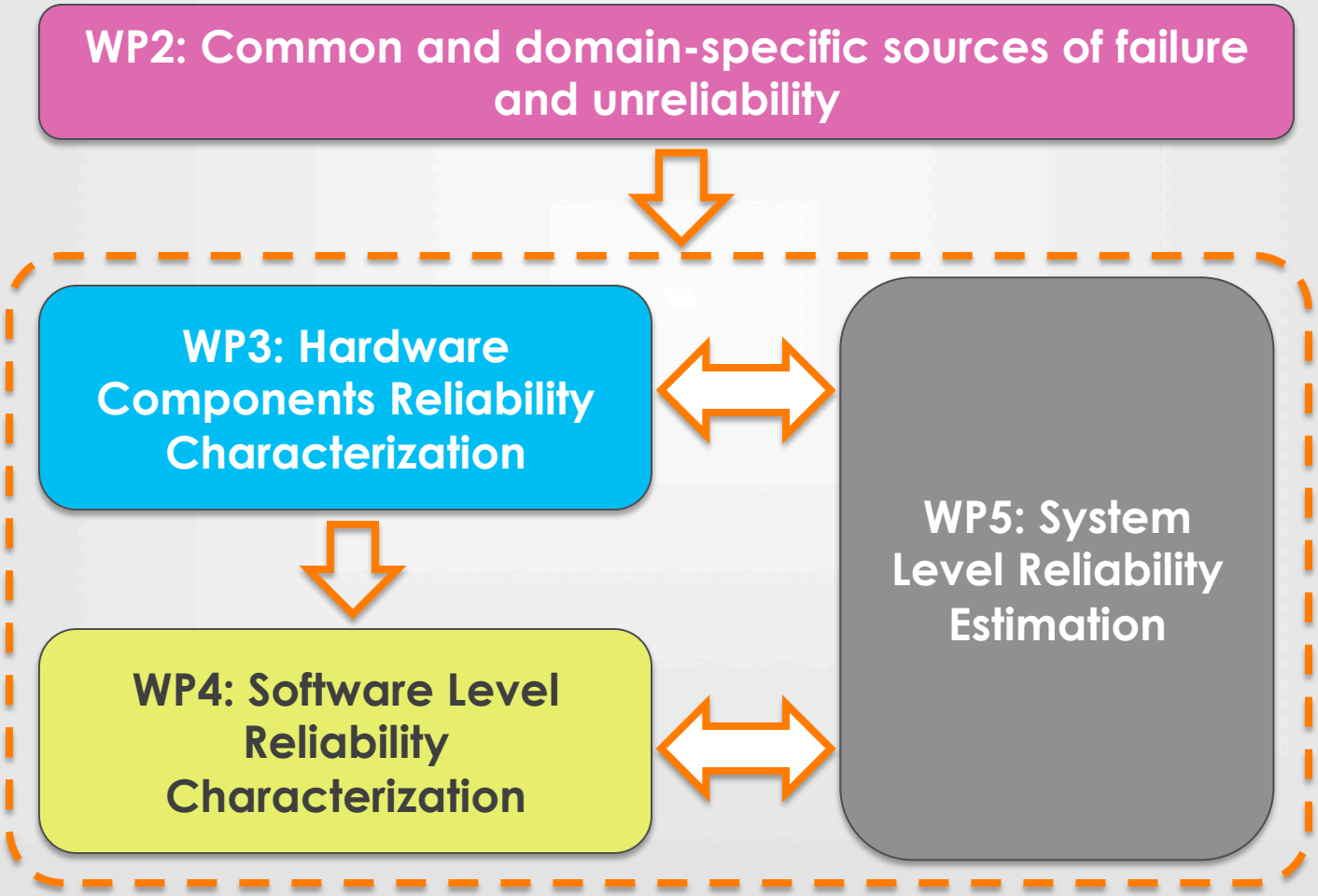
THE TECHNICAL ACTIVITIES



WP2: Common and domain-specific sources of failure and unreliability

- Analysis of the different **failure mechanisms** that will be relevant for the computing continuum (scaled bulk CMOS, III-V Ge, Finfets, spin logic, etc.)
- Identification and characterization of the **main sources of failure**
- **Reliability requirements** for the different computing segments within the computing continuum such as ES and HPC.
- Definition of the **different operating modes** of the system (e.g., voltage and frequency levels), and the different operating conditions (e.g., temperature, electronic noise, etc.) that may **affect reliability**

WP3: Hardware components reliability characterization

- The hardware of computing systems is iteratively broken down into its basic components and characterized form the reliability standpoint
  - Computation of specific parameters and measures potentially impacting the overall system reliability
- Classes of considered **hardware components**:
  - **CPUs**
  - **Memories** (e.g., DRAM, SRAM, Flash, RRAM, etc.)
  - **Accelerators** (e.g., GPUs)
  - **Peripherals**
  - **Interconnects**

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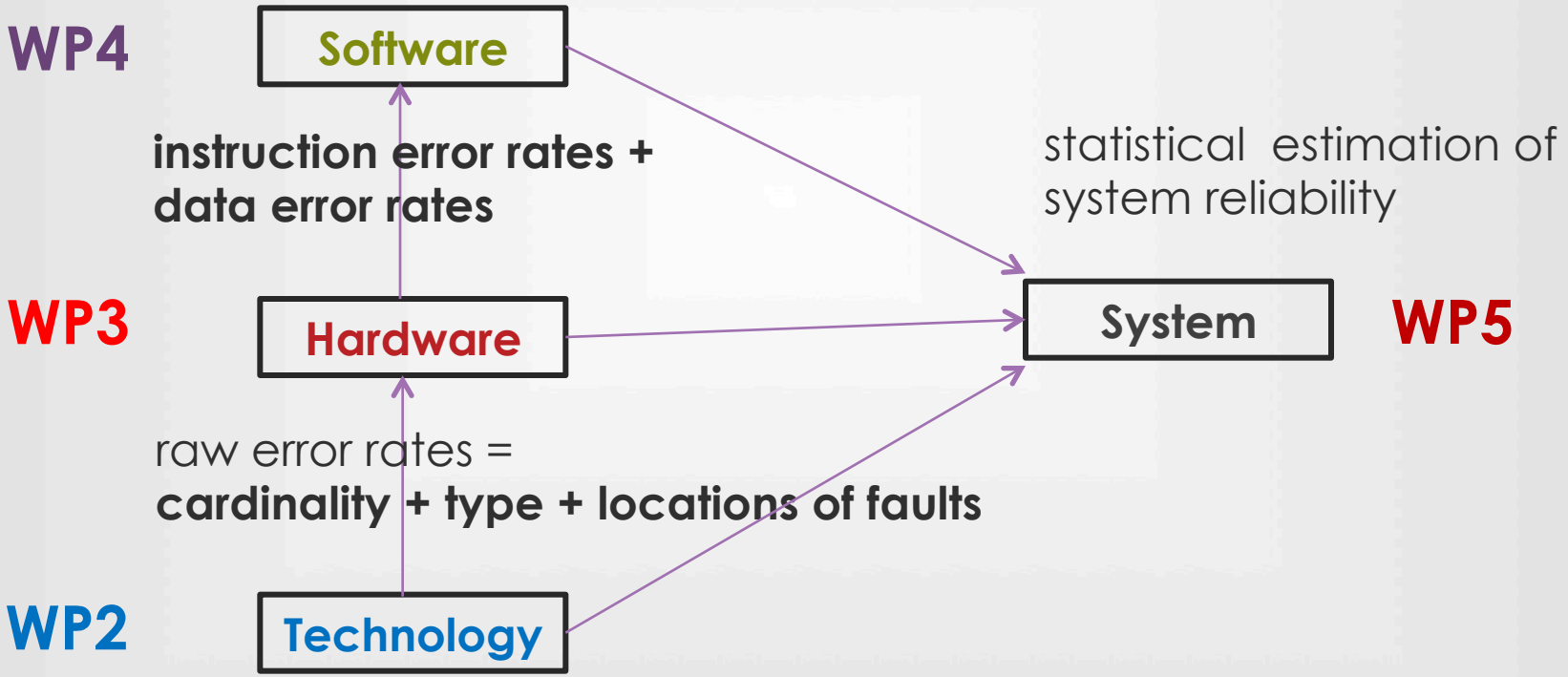
WP4: SW level reliability characterization

- The **software stack** is broken into its basic components (from high-level application software modules down to the instruction set architecture level) and **analyzes how hardware errors propagate through the software stack**
- To allow early reliability estimation when the hardware architecture is still not defined WP4 aims at defining metrics and models enabling to **abstract the behavior of the software from a specific hardware architecture**

WP5: System level estimation models

- Measures and analyses performed in WP3 and WP4 are **integrated into a comprehensive statistical framework able to estimate reliability** metrics defined in WP2 (iteratively in the different design stages of the system)
- Estimated reliability metrics are used to **develop algorithms able to support the designers in the reliability related decision-making process** that will in turn allow the design of reliable systems with improved cost-related characteristics (area, energy/ power, and performance) and reduced TTM)

LINKS AMONG DIFFERENT SYSTEM LAYERS (WPs)



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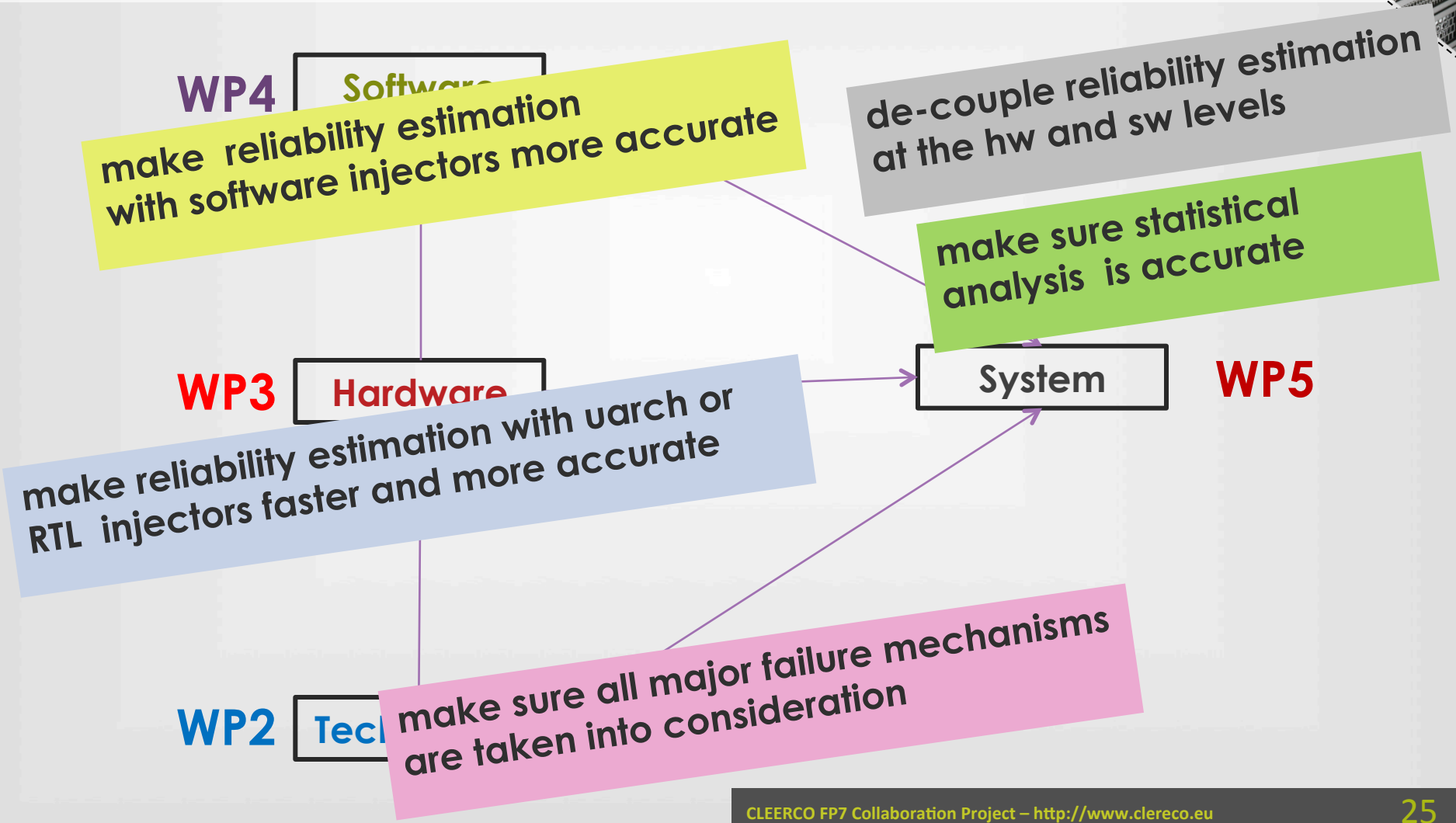
MAJOR RESEARCH CHALLENGES



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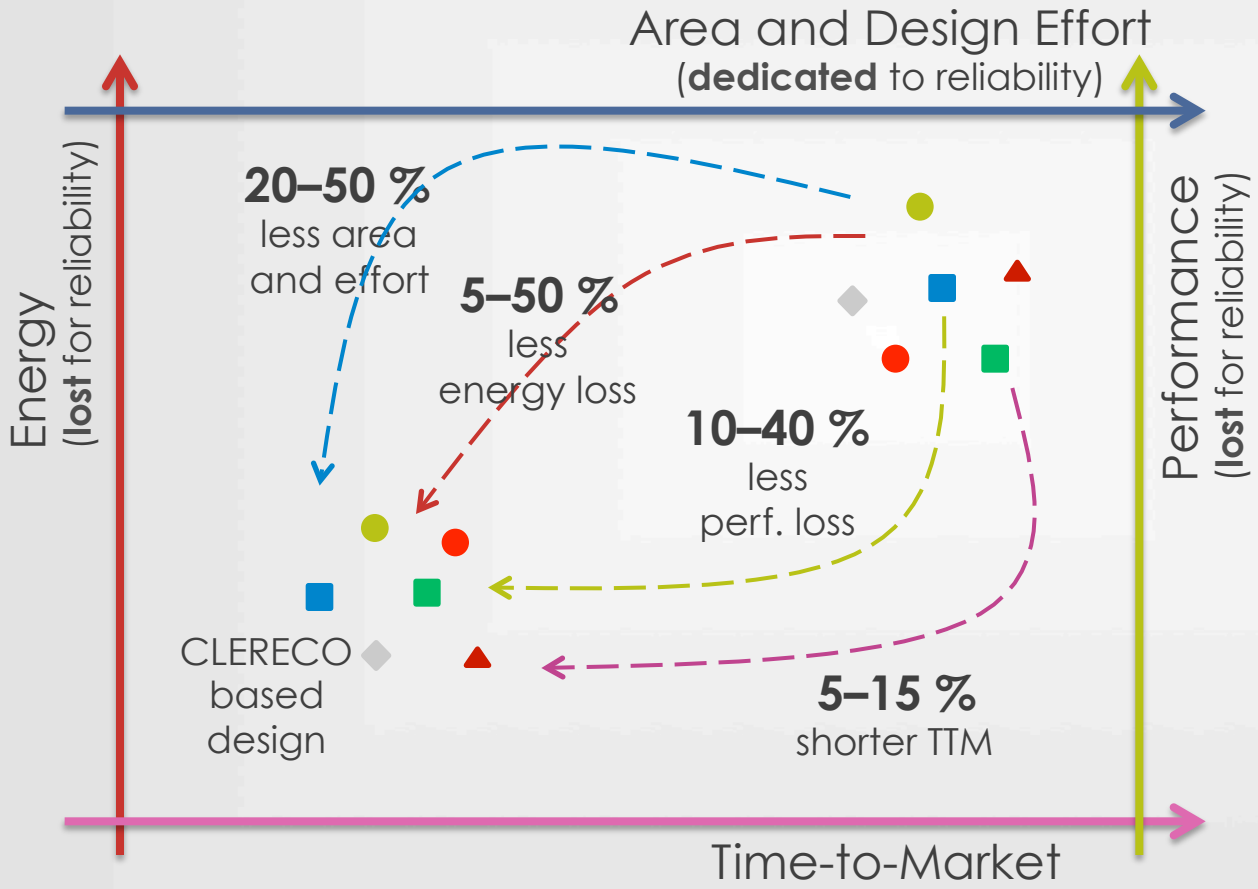
BENEFITS IN SYSTEM-DESIGN



Different points correspond to different segments of computing systems market.
Percentage improvements will vary depending on each market's primary optimization points.

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CONCLUSIONS

- The characteristics that **CLERECO** pursues for its reliability-evaluation framework are:
  - **Flexibility**: reliability analysis must be possible starting from the very early design stages
  - **Speed**: time-consuming simulations and/or fault-injection campaigns must be avoided and replaced by accurate statistical models and procedures
  - **Accuracy**: reliability estimations must be as precise as possible.
  - **Comprehensiveness**: a heterogeneous set of target systems must be analyzable ranging from very application-dependent ES to more general-purpose HPC systems

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Thank you.