STT-MRAM Reliability Estimation at Block-level Granularity

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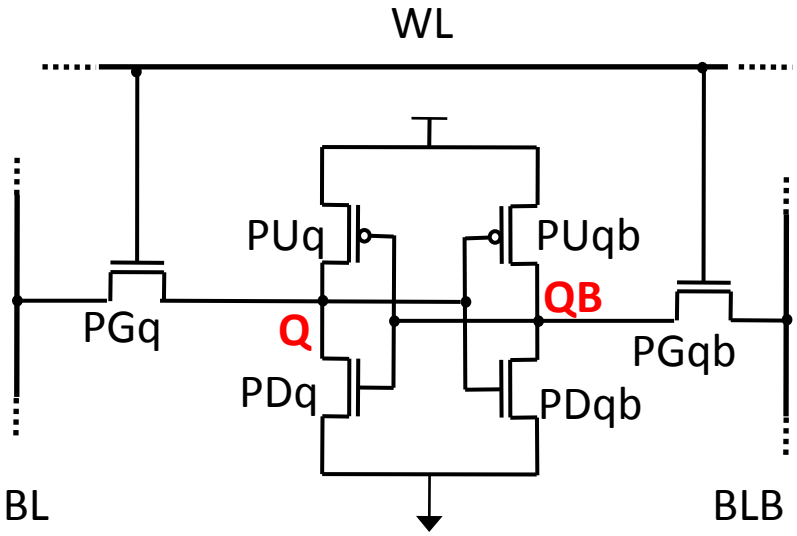
Motivation

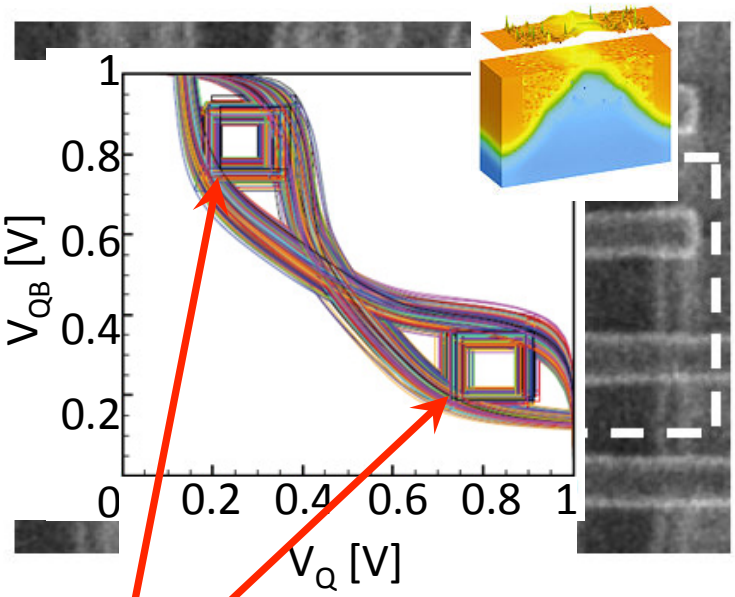
Memories Today

	SRAM	DRAM	NOR-Flash	NAND-Flash
Cell Size	$120F^2$	$4\text{-}6F^2$	$10\ F^2$	$4\text{-}5\ F^2$
Read Latency	<1ns	20ns	5,000ns	25,000ns
Write Latency	<1ns	20ns	1,000,000ns	200,000ns
Static power	YES	YES	NO	NO
Endurance	$>10^{15}$	$>10^{15}$	10^4	10^4
Non-volatility	NO	NO	YES	YES

Motivation

SRAM Memories

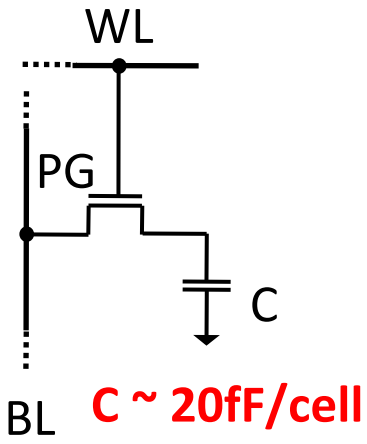




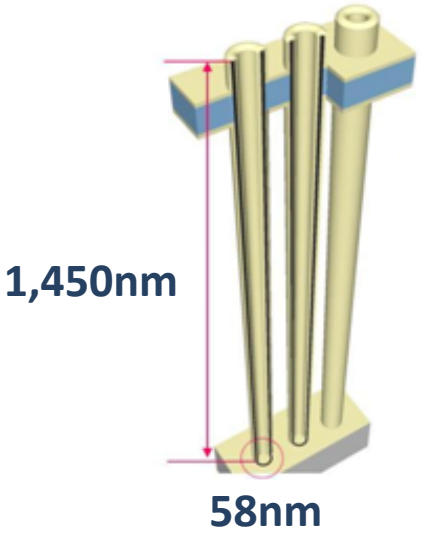
SNM – Static Noise Margin

Motivation & Goal

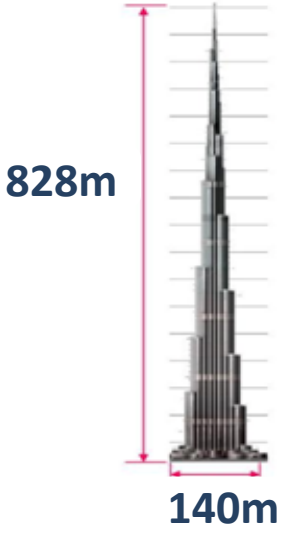
DRAM Memories



C ~ 20fF/cell



Aspect ratio: 25

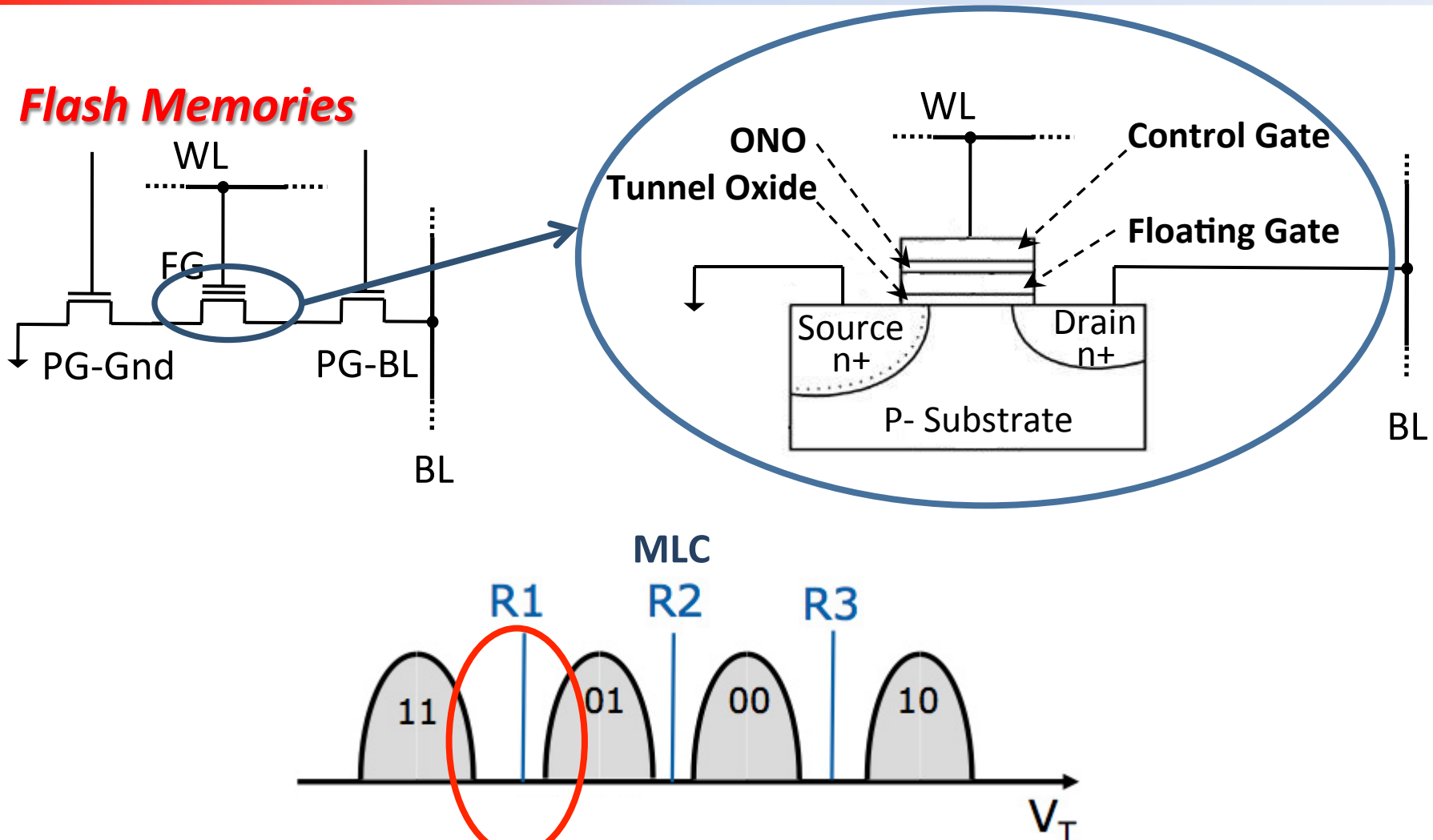


Aspect ratio: 6

- Very high-k materials (k = the dielectric constant)
- Very tall structures

Motivation & Goal

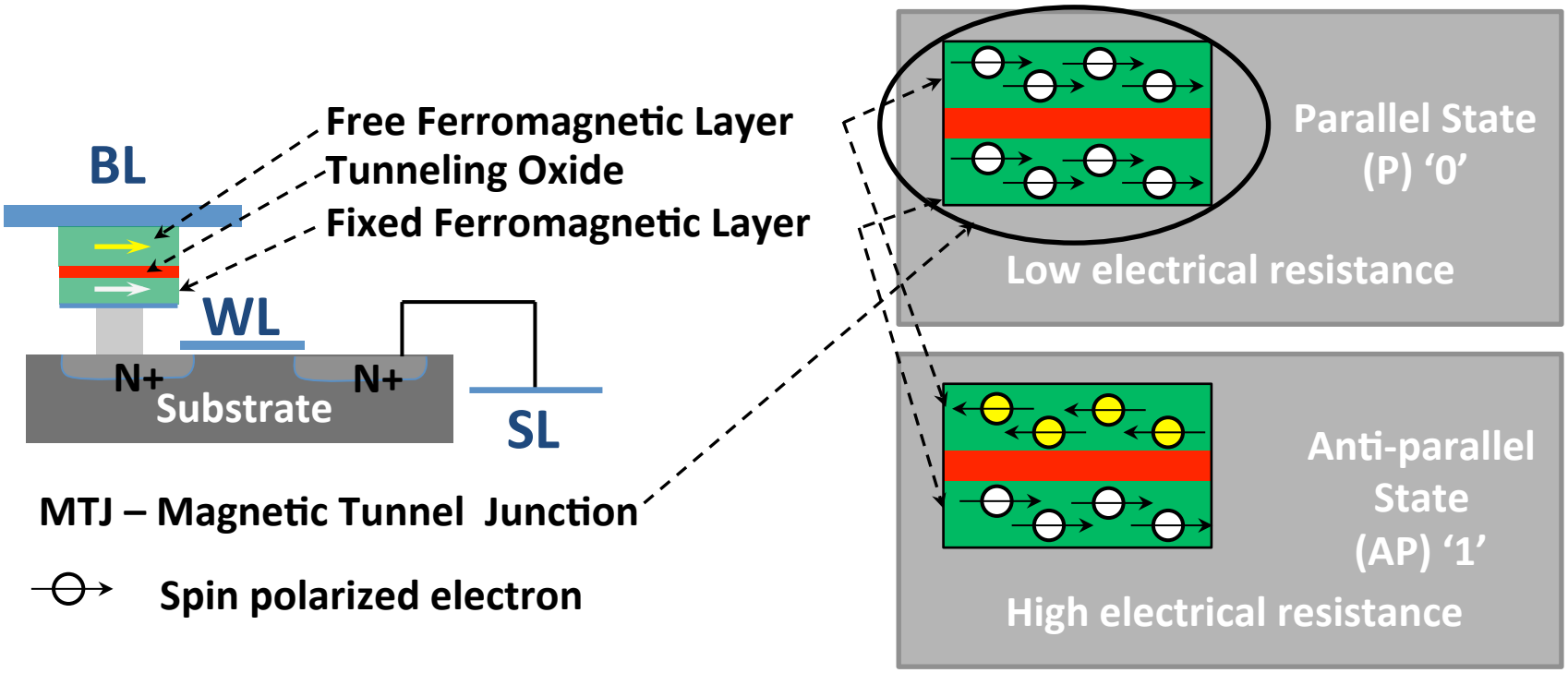
Flash Memories



Outline

- Spin Transfer Torque (STT) MRAM
  - Operation Mode
  - Electrical Model
  - Reliability Issues
- STT-MRAM Block Reliability Estimation
  - Methodology
  - Simulation Results
- Discussions
- Conclusions

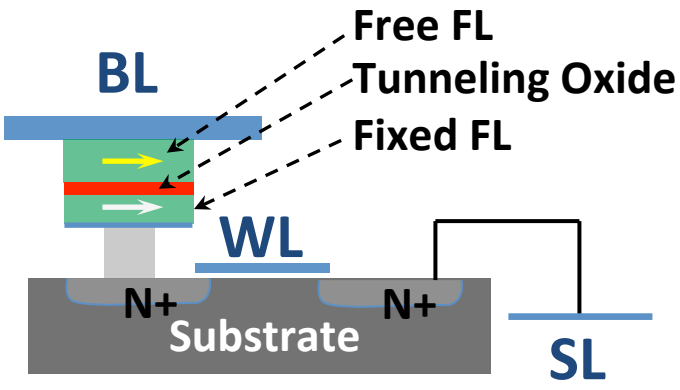
STT-MRAM
Operation Principle



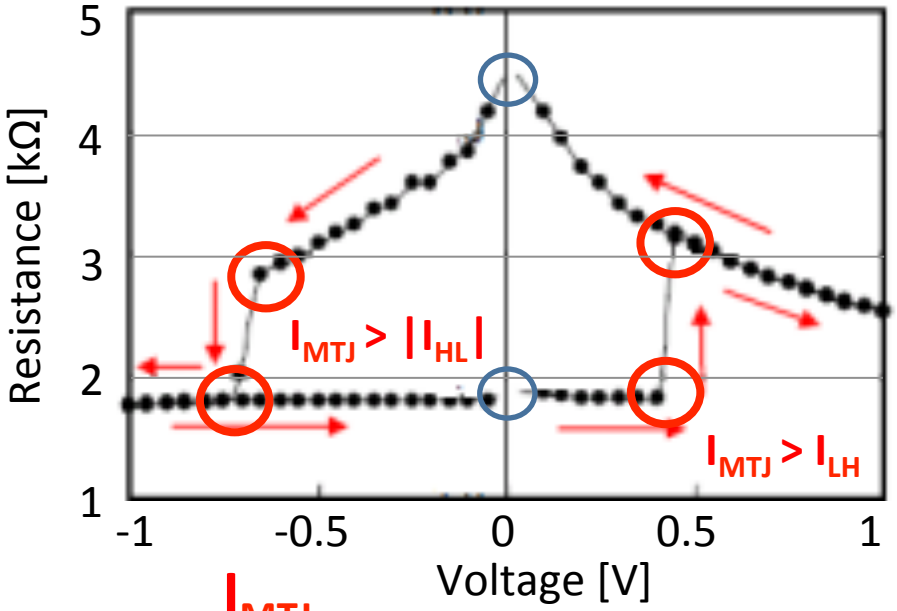
The orientation of the free layer:

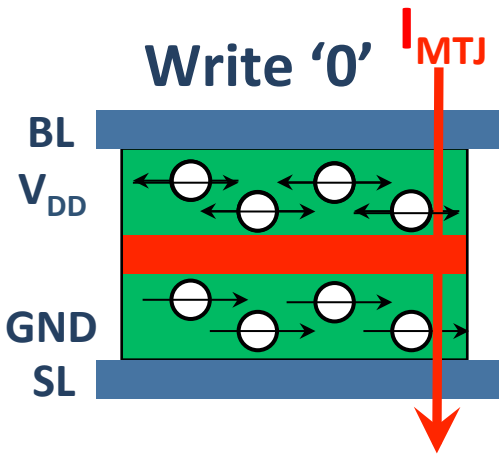
- determines the *resistance* of the material
- can be changed by injecting *current.*

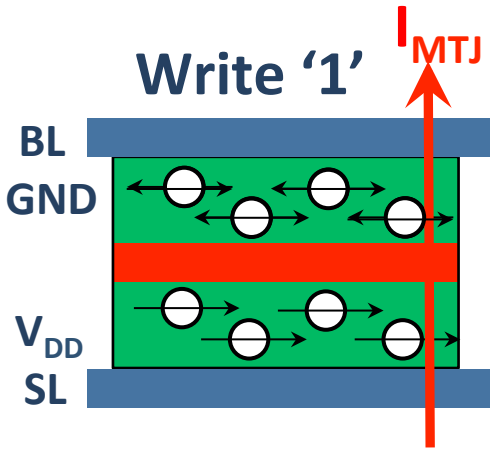
STT-MRAM
Electrical Model



FL – Ferromagnetic Layer





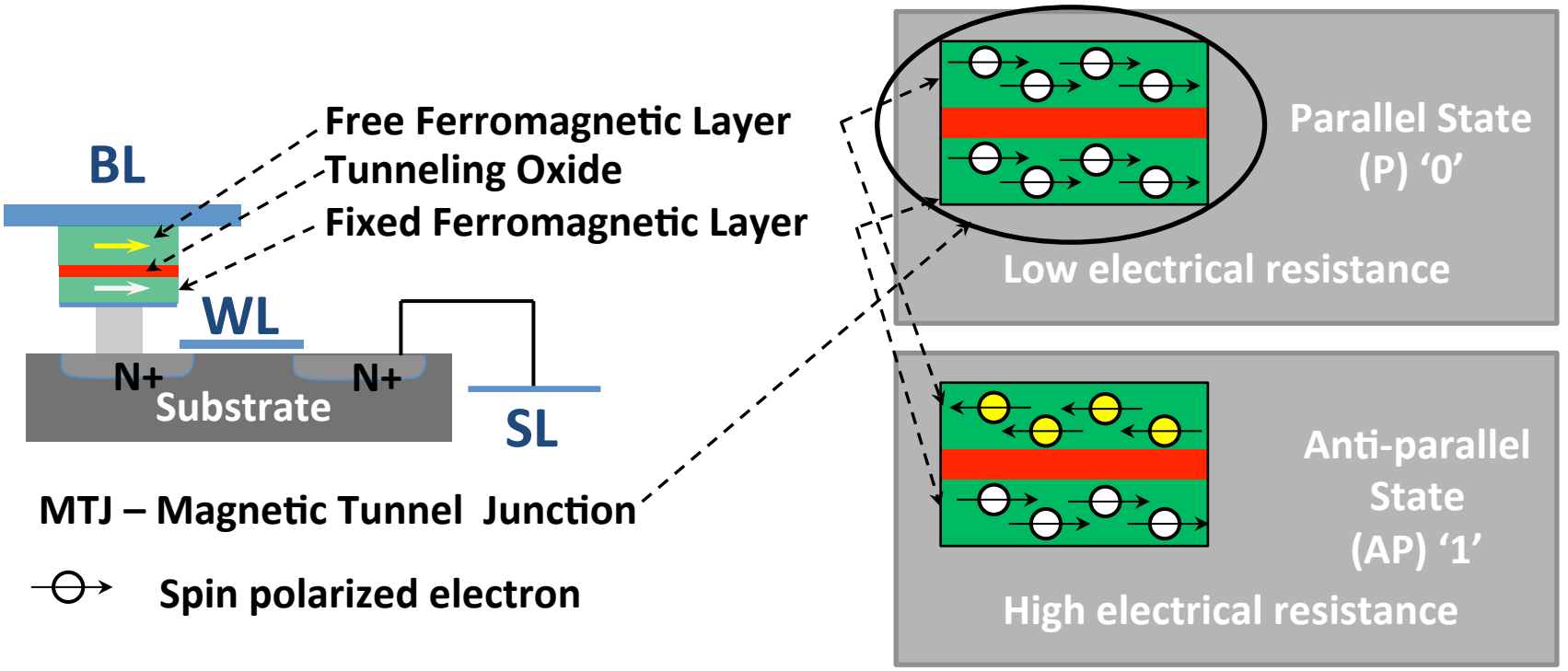


I_{HL} –high to low transition

I_{LH} –low to high transition

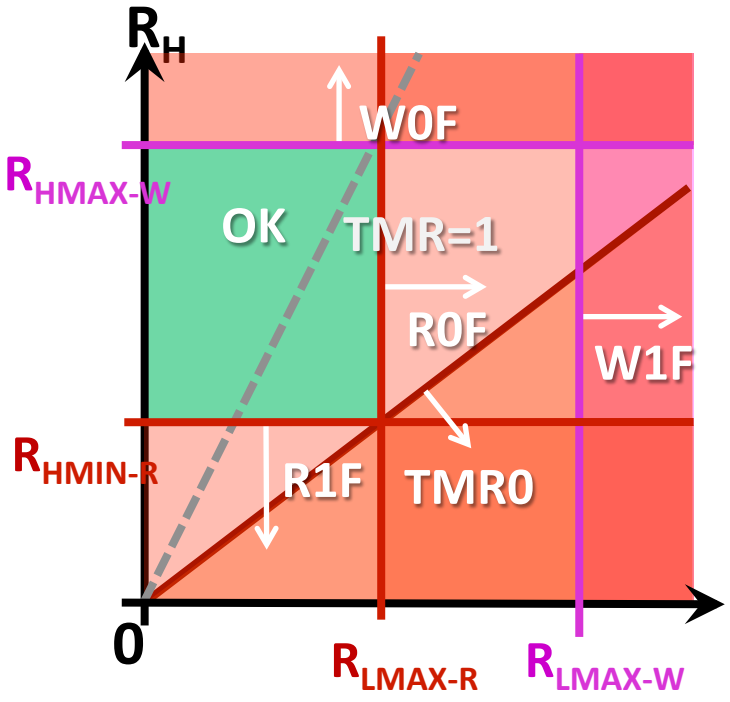
[M. Hosomi, IDEM, 2005]

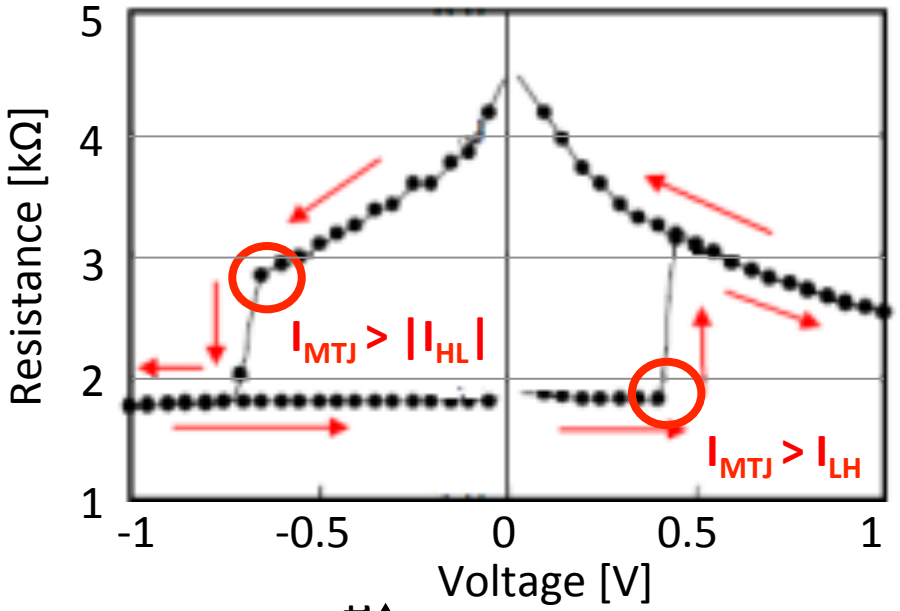
STT-MRAM
Reliability Issues

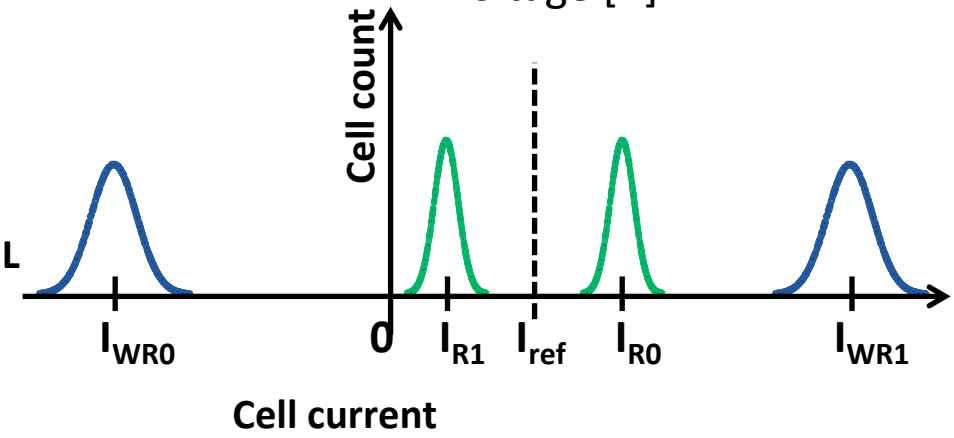


- Tunneling oxide thickness and cross-section area
- Free layer thickness

STT-MRAM
Cell Reliability Evaluation







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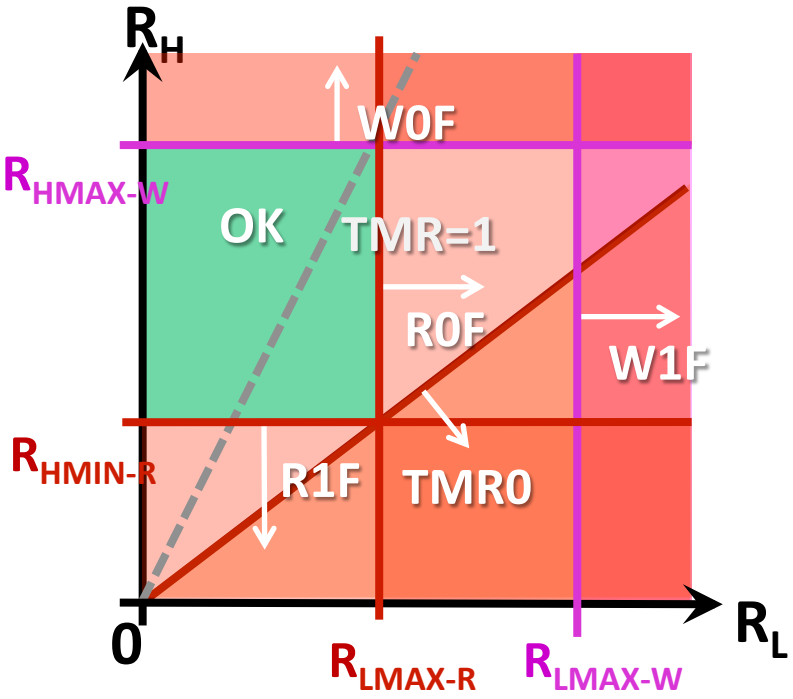
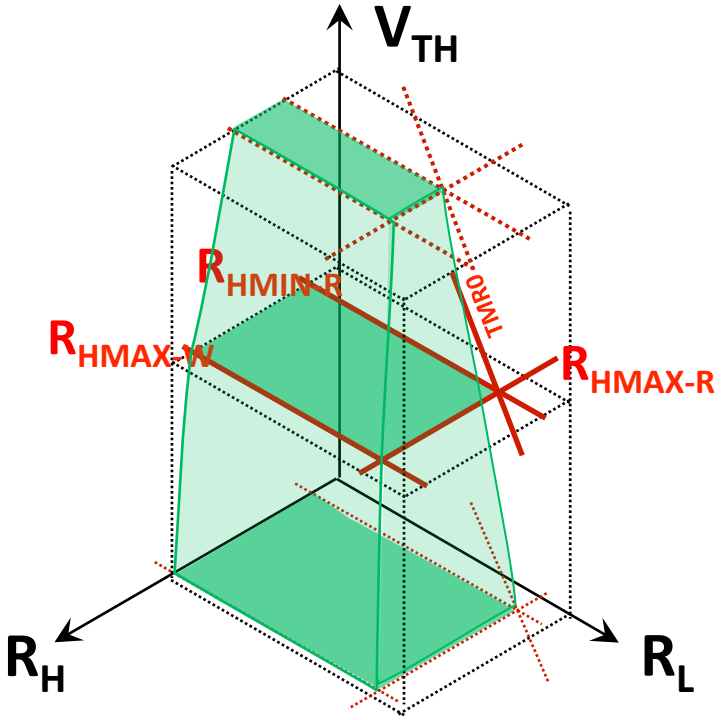
Cell Reliability Evaluation





STT-MRAM

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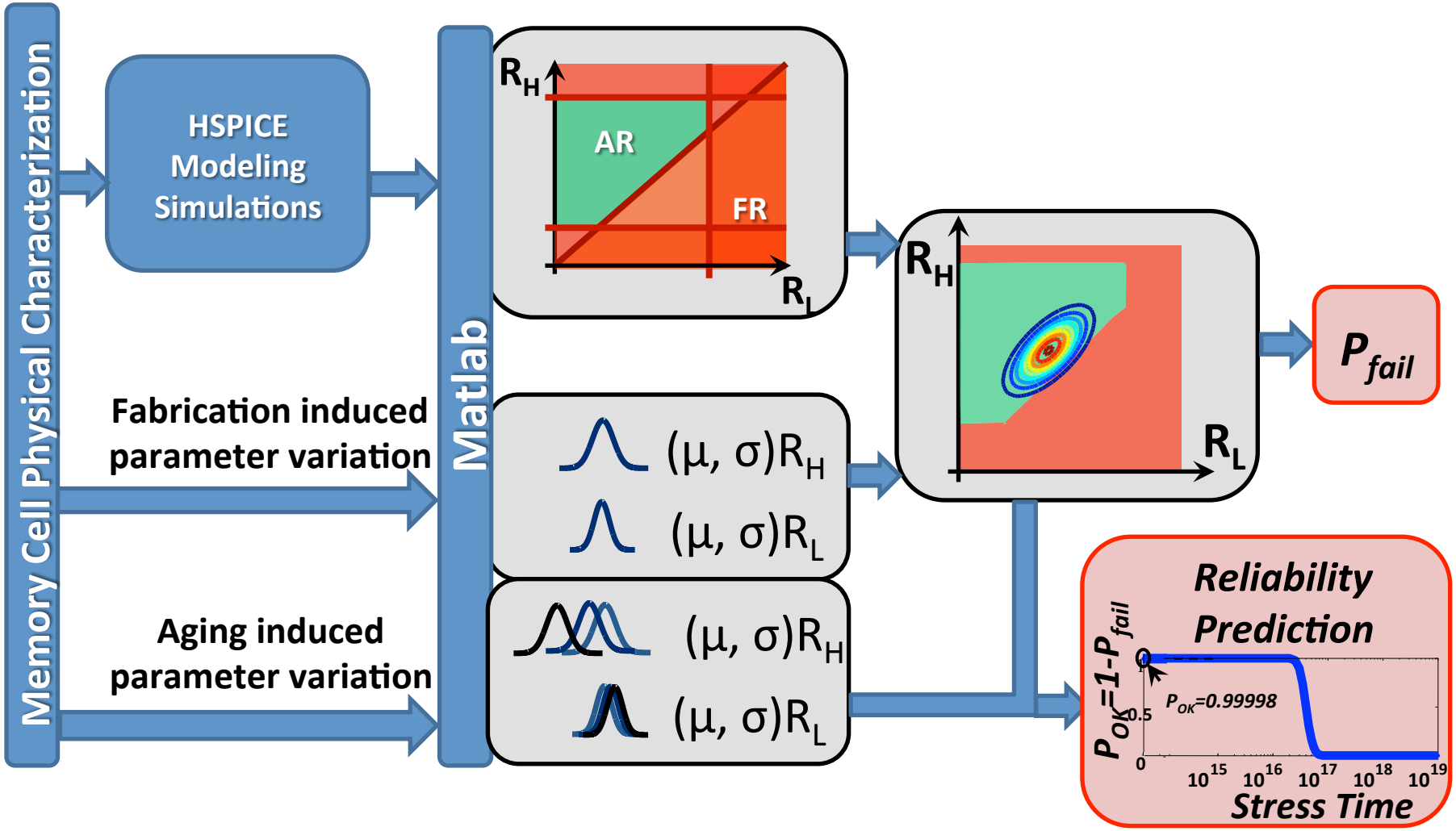

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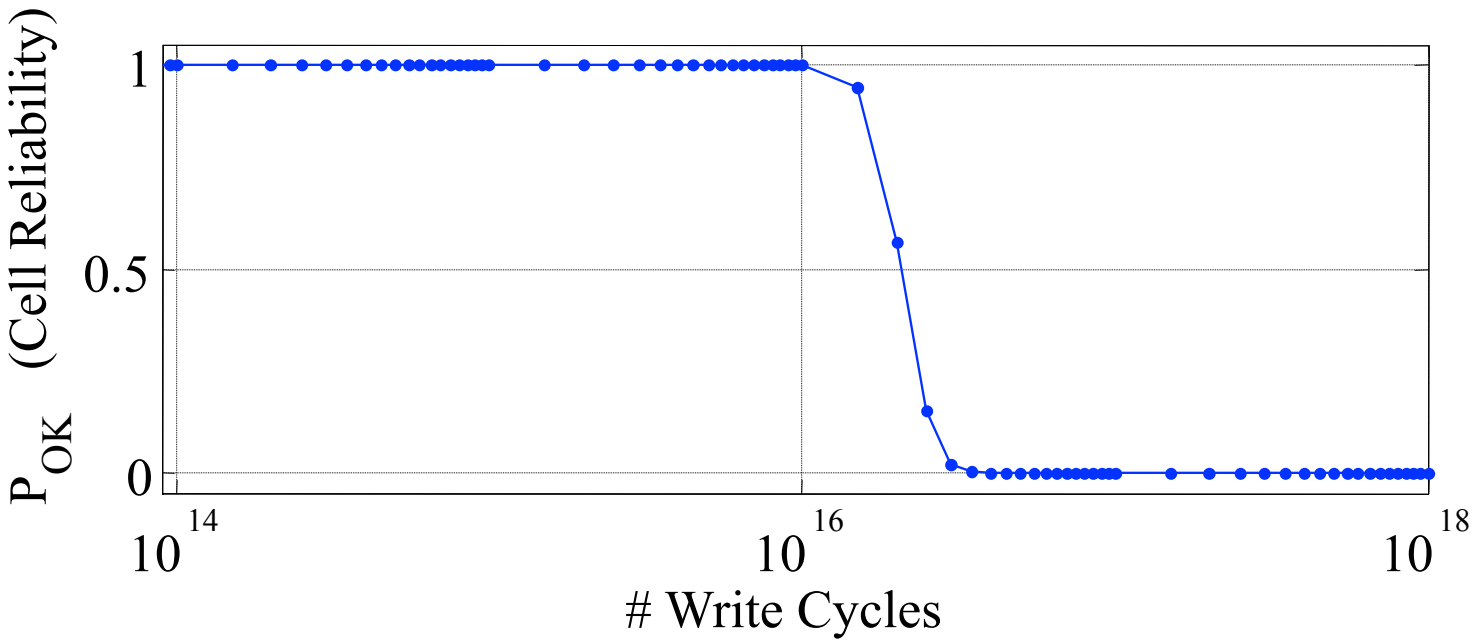
Cell Reliability Evaluation



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Block Reliability Estimation
Methodology

- **Assumptions:**
  - **Stress lifetime (n_{BC}) measured in block cycles**
  - **Block usage is stationary**
  - **Assume known activity spread throughout the block**
  - **The access rate (γ_i) of each word (w_i) with $i=1:B$ is a fraction of the block cycle.**

$$R_{block}(n_{BC}) = \prod_{i=1}^{B}\left[R_{cell}\left(\gamma_i \cdot n_{BC}\right)\right]^N$$

$[R_{cell}(\gamma_i\, n_{BC})]^N$ is the reliability of word w_i after n_{BC} block cycles

Block Reliability Estimation
Methodology – Extreme Cases

- ***Maximum*** **Localized Access (worst case)**
  - **All access operations on the same word**

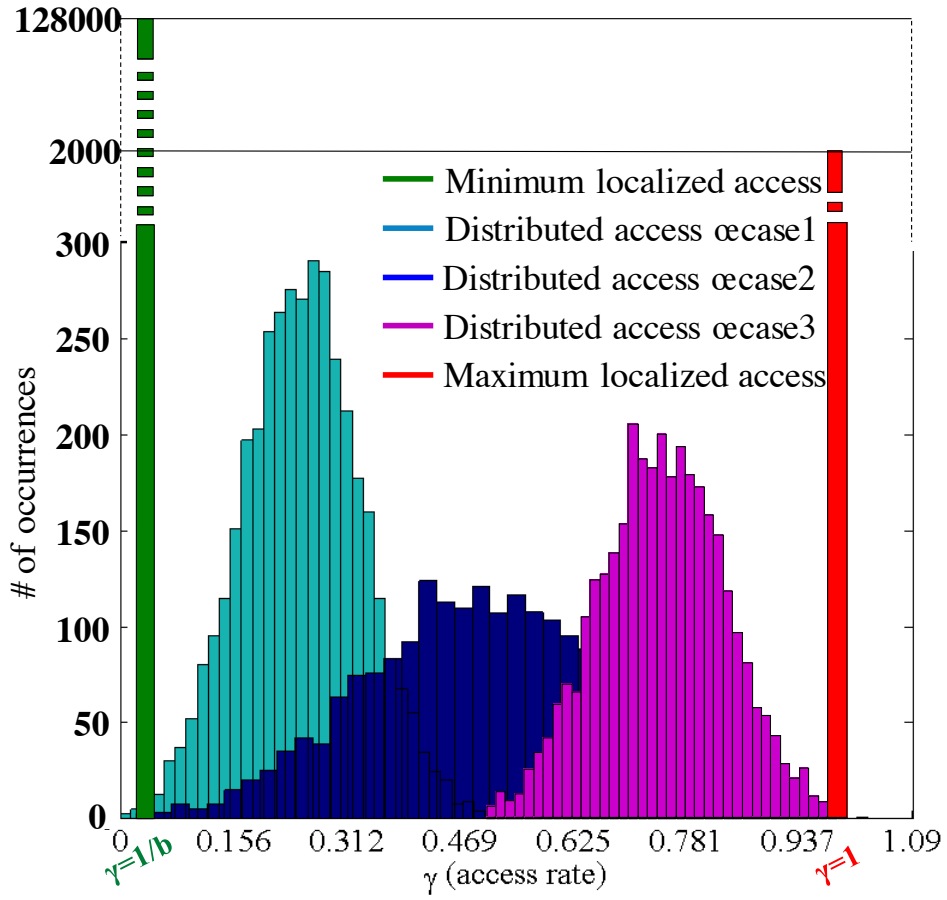
$$R_{block}(n_{BC}) = [R_{cell}(\gamma_1 \cdot n_{BC})]^N \cdot \prod_{j=2}^{B}[R_{cell}(\gamma_j \cdot n_{BC})]^N$$

- ***Minimum*** **Localized Access (best case)**
  - **All words are equally accessed**

$$R_{block}(n_{BC}) = \left[R_{cell}\left(\frac{1}{B} \cdot n_{BC}\right)\right]^{B \cdot N}$$

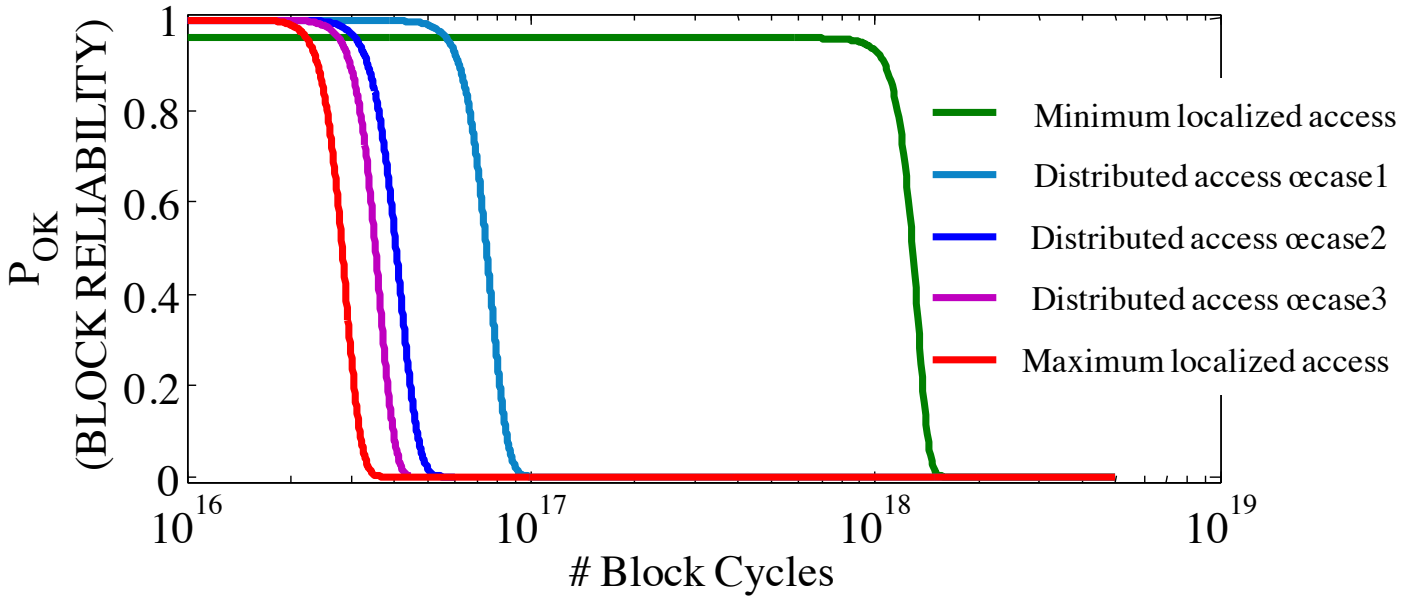
Block Reliability Estimation

Simulation Results



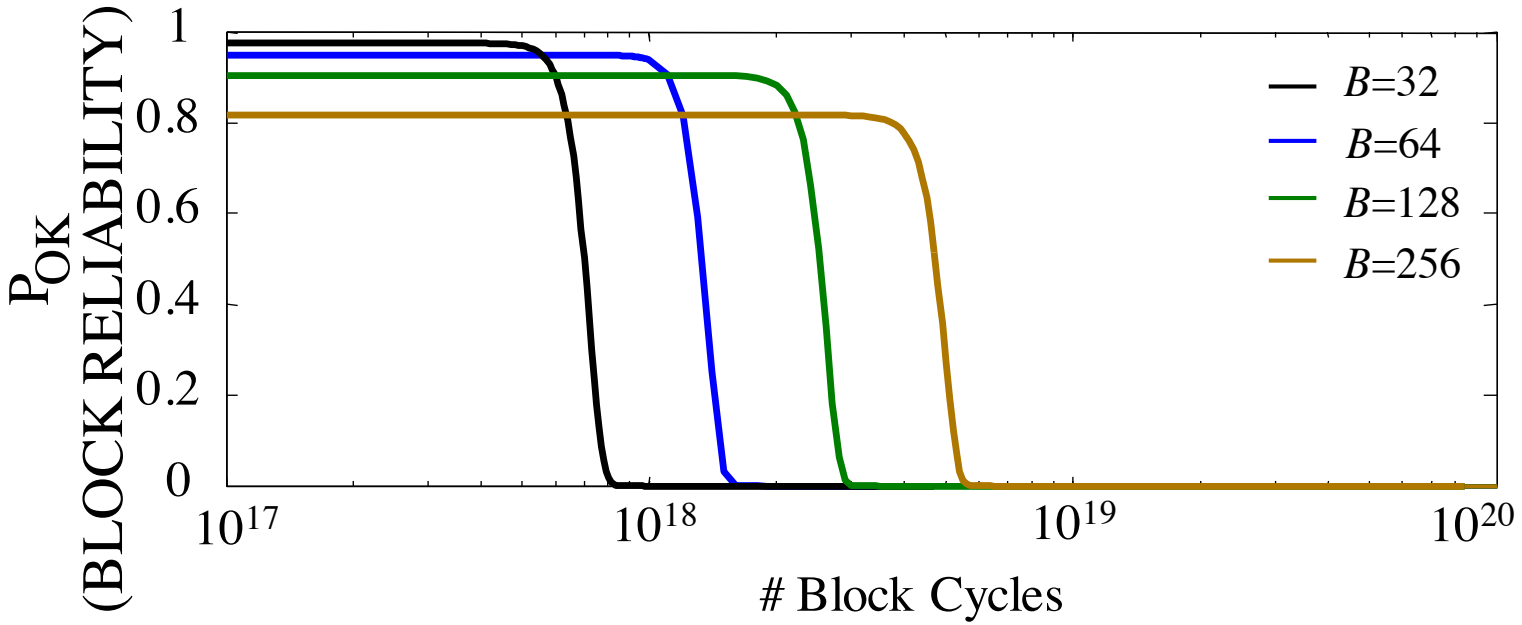
Block Reliability Estimation

Simulation Results



Block Reliability Estimation

Simulation Results



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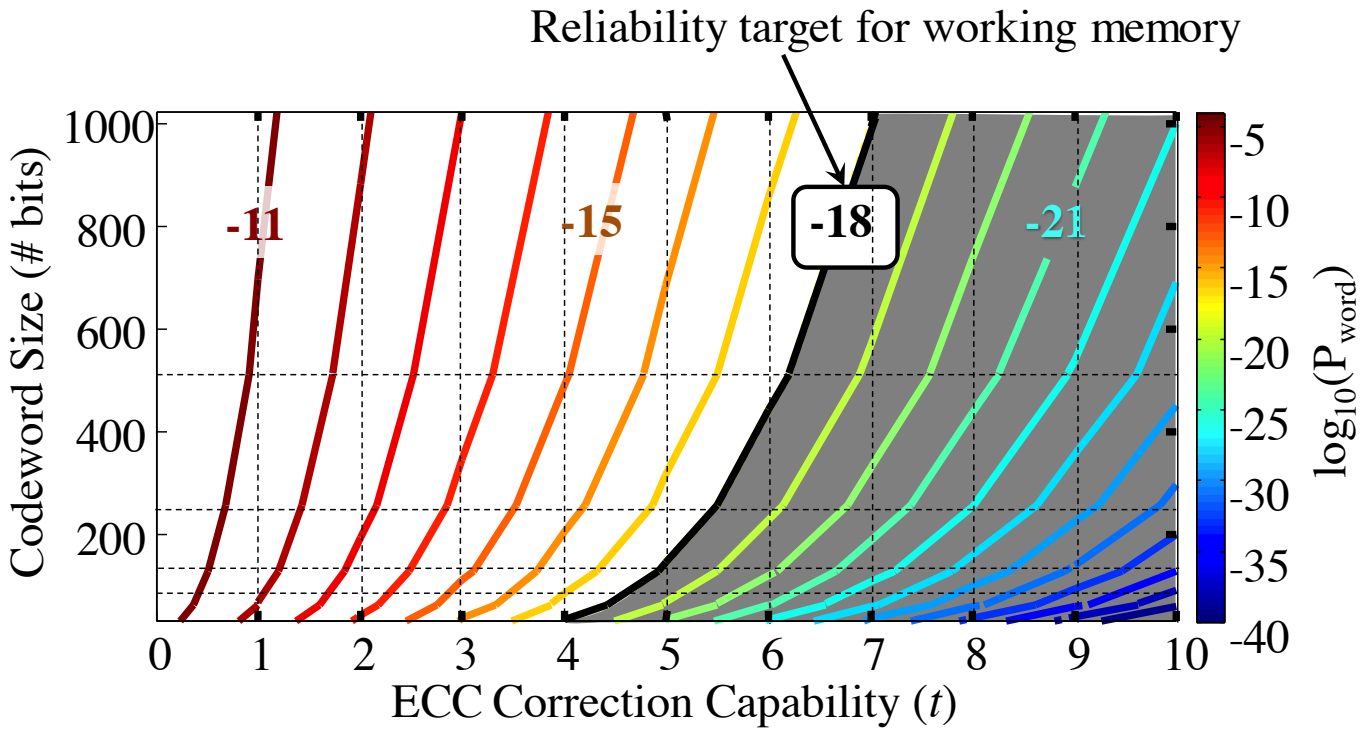
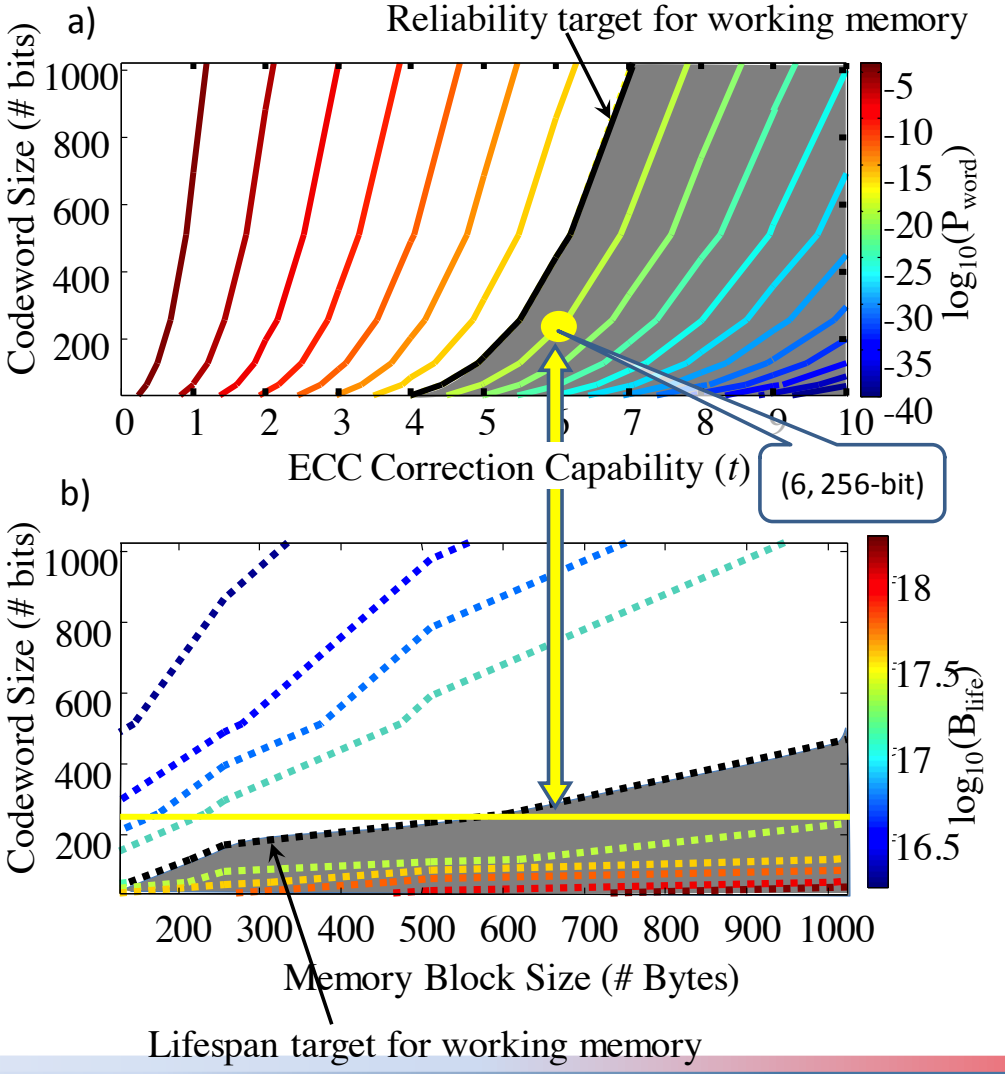
Discussions on ECCs



Discussions on ECCs



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Conclusions

- **Carefully controlling the access rate of a memory word, the lifespan of the entire memory block can be substantially increased.**
- **Large block size means longer lifespan, but less reliable device**

Conclusions

- Methodology for STT-MRAM reliability prediction at block level
  - general: applicable to a range of memory topologies
  - fast: variability induced degradation is evaluated with reduced number of simulations
  - comprehensive: allows for fresh and aged cell/ block reliability estimation with different usage scenarios

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