The uncertainty of technology and its consequences

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Motivation

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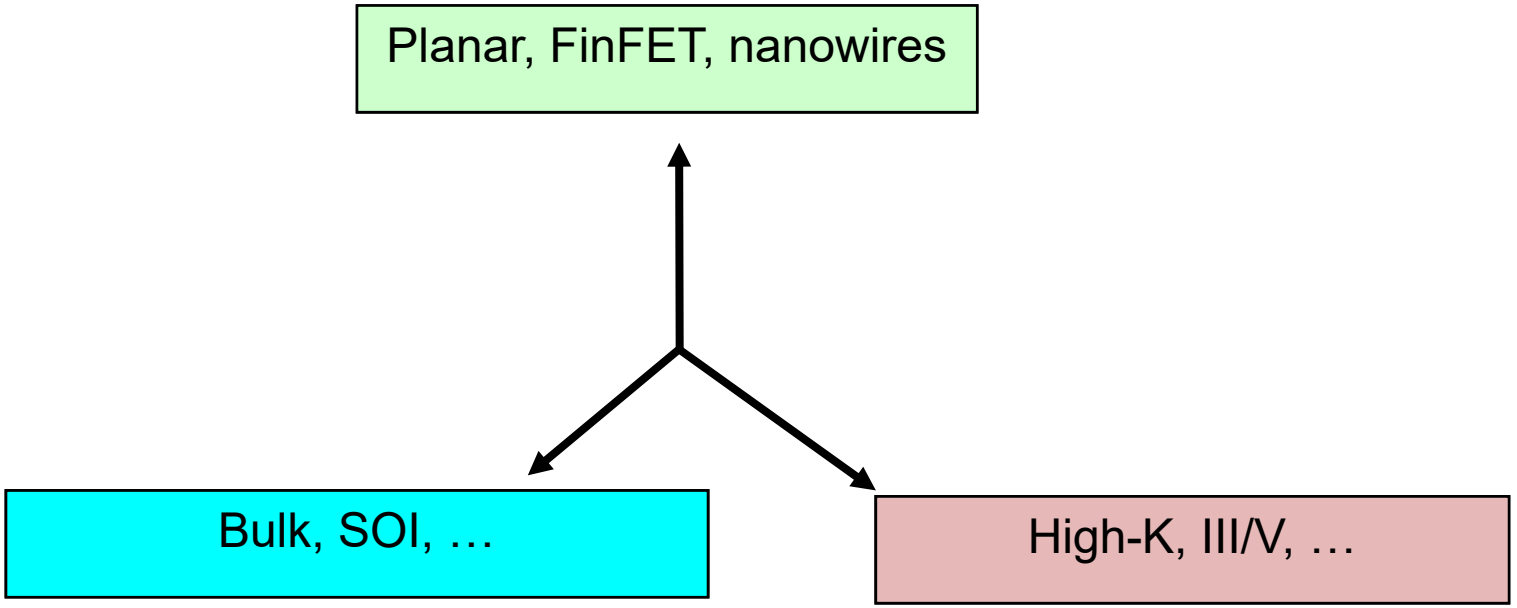
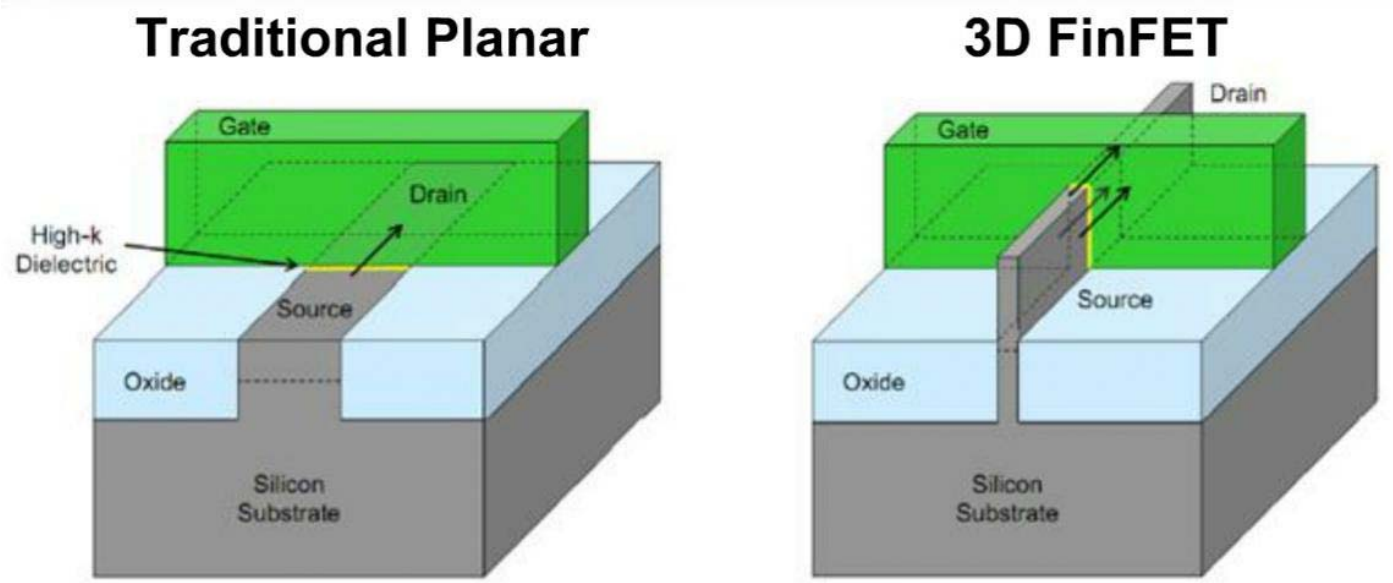


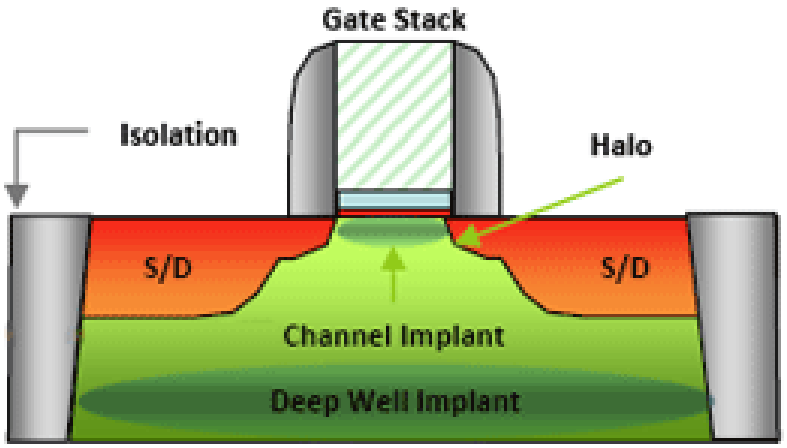
- **Rapid change in silicon technology**
  - **Characterize the effects on memories and logic**
    - **Delay, Power and Robustness**

Motivation - Examples

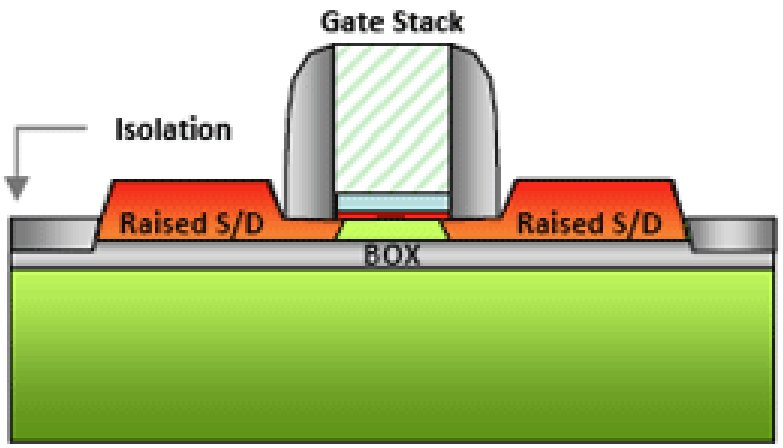


- **FinFET / Planar (bulk)**
  - **Variability (FinFET "eliminates" RDF but …)**
  - **Leakage (FinFET reduced up to 10% or less)**
- **FinFET / Planar (FD-SOI)** (source: Applied Materials)
  - **Just about the same perf. but FinFET on top**
  - **FD-SOI less process steps (i.e. cheaper)**

Motivation - Examples



Bulk Device

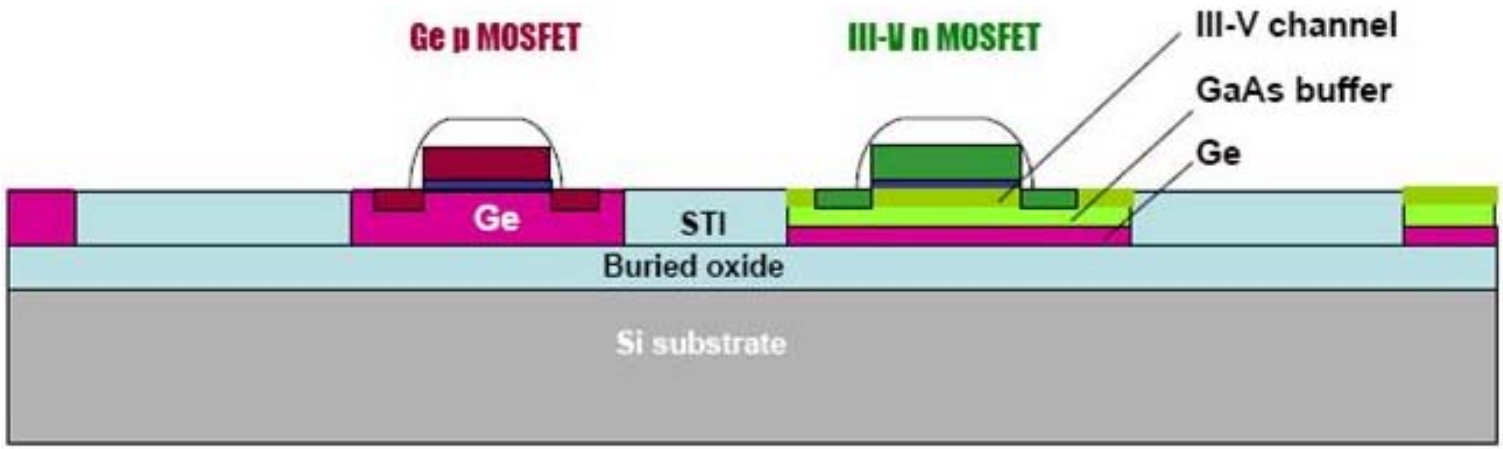


FD-SOI Device

- **SOI / Bulk[1]**
  - **Variability (Bulk ~ 2.5x SOI)**
  - **Cost (SOI cheaper, less process steps)**
  - **Endurance (harsh environments)**

[1]Comparison study of FinFETs: SOI vs. Bulk Performance, Manufacturing Variability and Cost. D. Fried (IBM), T. Hoffmann (IMEC), BY Nguyen (SOITEC) S. Samavedam (Freescale), H. Mendéz (SOI consortium)

Motivation - Examples

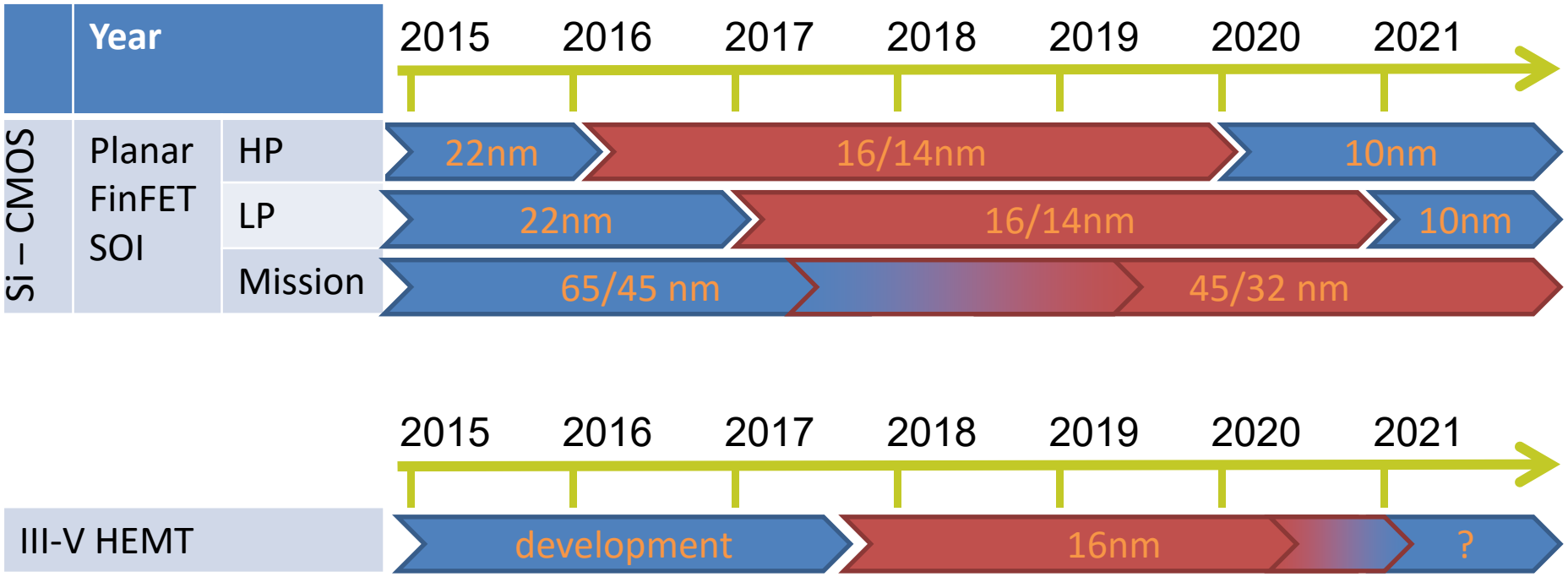


- **III/V + FinFET**
  - **25% performance increase at same power level[1]**
- **III/V + vertical FETs or nanowires**
  - **Currently under strong research efforts**

[1]"Logic scaling beyond 10nm, a power-performance-area-cost trade off" An Steegen, IMEC senior vice president process technology, IMEC International Technology Forum, Nov. 2013

Motivation

- **Gradual change of technology (ITRS+others)**

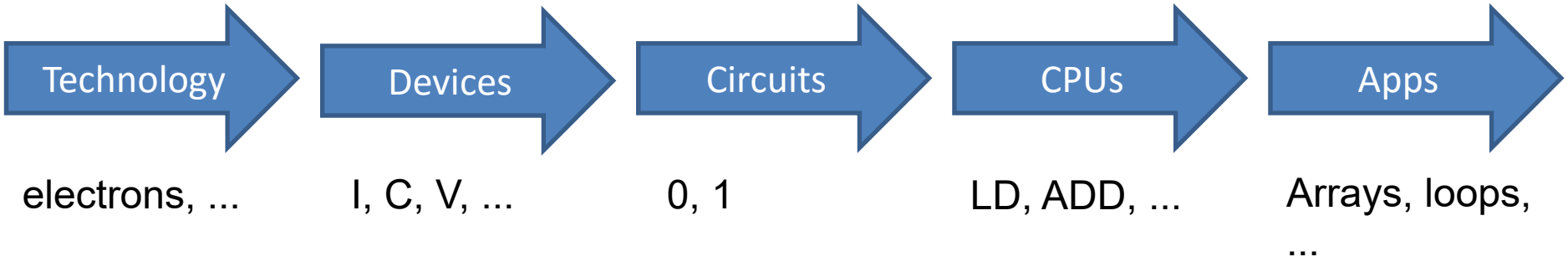


What should we aim for

- **Reduce the device to system characterization**
  - **Define cross-layer interfaces**
    - **vulnerability factors, probability of failure, …**
  - **Speed-up the computation of metrics**
    - **Statistical models, IA techniques**
- **Avoid worst-case design.**
  - **Incorporate masking effects.**
  - **Incorporate usage effects (i.e. degradation)**

Positive Side-effects

- **Feedback loop made a reality**



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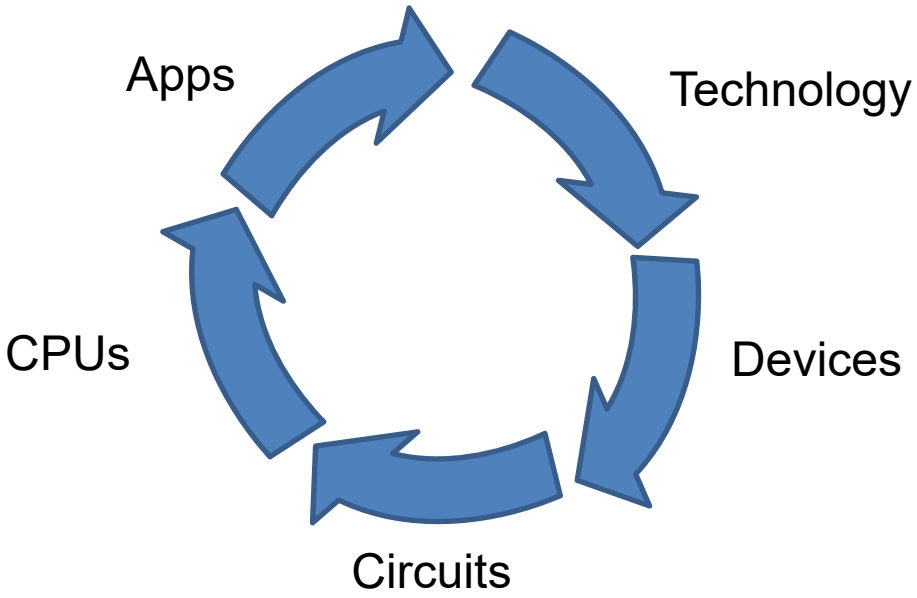

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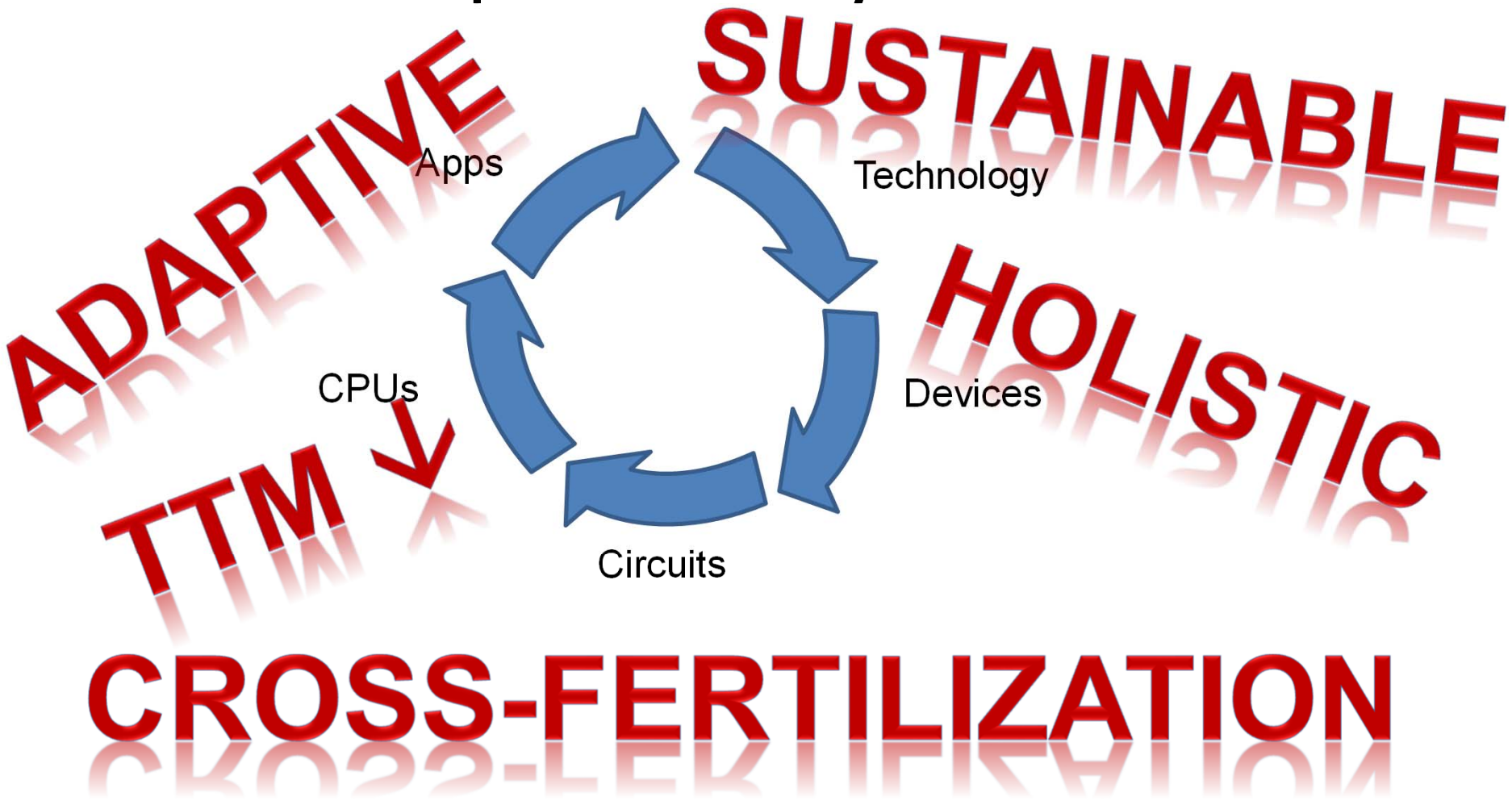

Answers for old questions

- **When running “Angry birds” will I see a performance difference with a:**
  - **10% higher fin height**
  - **III/V transistor**
  - **new memory cell**
  - **super-cool ECC code**

First steps @UPC

- **At the circuit – CPU level**
  - **Energy/Delay/Robustness modelling and tools**
  - **Definition of realistic scenarios (i.e. HPC, SoC, embedded)**

- **Results so far**
  - **Integrated Framework (e.g. INFORMER)**
  - **Probability of failure estimation through statistic methods (e.g. SSFB, REEM)**
  - **Integrated circuit-CPU techniques (e.g. iRMW)**

Next steps (broader scope)

- **Define interfaces at different levels**
- **Integrate with OS/applications**
- **Speed-up characterization/modelling/estimation at all levels**
- **Find NEW cross-layer solutions**

Conclusions

- **Not predictable technology characteristics**
- **Fast technology to system communication needed**
- **Need to define interfaces between layers**
- **Need to define better models and techniques**

A reasonable estimation is better than no estimation

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