Integration of STT-MRAM model into CACTI simulator

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CACTI Simulator

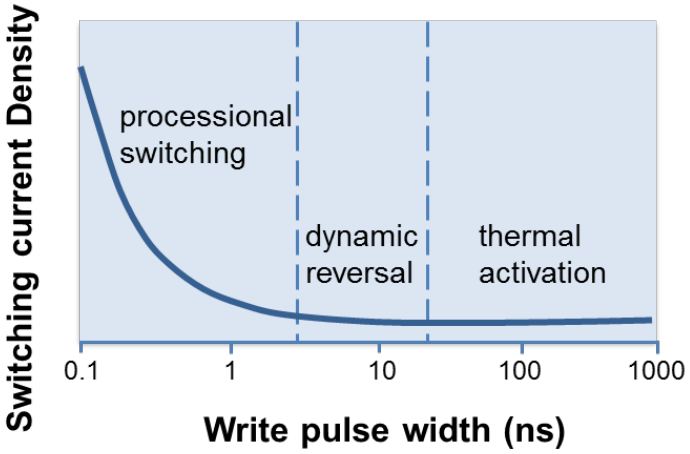
- Open-source high level cache and memory modeling tool;
- Embedded models for memory basic building blocks;
- Can evaluate: delay, power, area;
- Design space exploration to identify an optimum configuration (array size and chip interconnect) to meet the input constraints.

MTJ in CACTI Simulator

MTJ Parameter	Description
STT-Type	In-plane
J_{c0}	Critical current density
Δ	Thermal stability factor
R_L	MTJ resistance in parallel magnetization
R_H	MTJ resistance in anti-parallel magnetization
VBL	Bit-line voltage during write
R_{NMOS}	Equivalent resistance of the access NMOS

MTJ in CACTI Simulator

Write operation



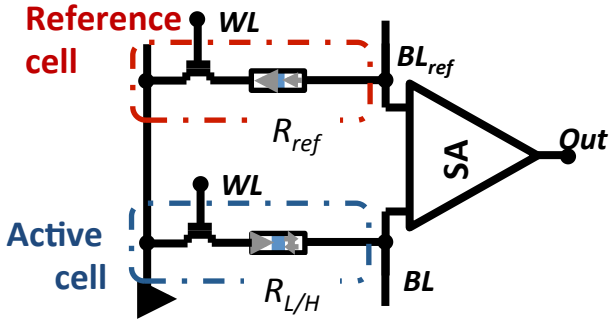
$\tau < 3ns \quad J_{c,PR}(\tau) = J_{c0} + \frac{C}{\tau^{V}}$

$3ns < \tau < 20ns \quad J_{c,DY}(\tau) = \frac{J_{c,TH}(\tau) + J_{c,PR}(\tau) e^{-k(\tau-\tau_c)}}{1 + e^{-k(\tau-\tau_c)}}$

$\tau > 20ns \quad J_{c,TH}(\tau) = J_{c0}\{1 - \left(\frac{1}{\Delta}\right) \ln\left(\frac{\tau}{\tau_0}\right)\}$

$$E_{write} = \frac{V_{write}^2}{R_{MTJ} + R_{ACC}} \tau_{write} + C_{tot} V_{write}^2$$

Read operation

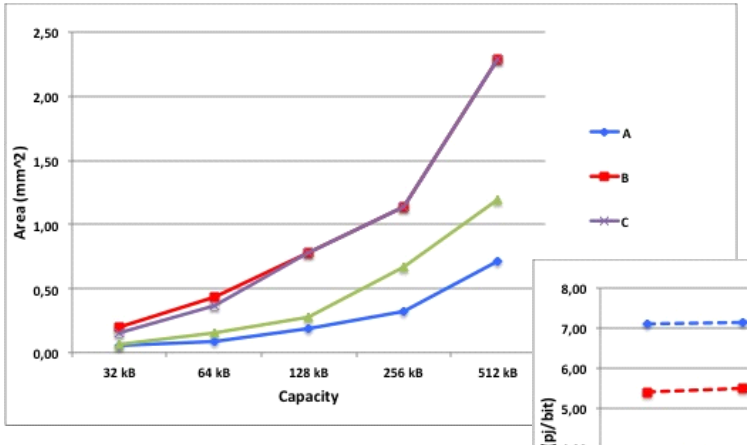


$$E_{read} = C_{tot} V_{read}^2$$

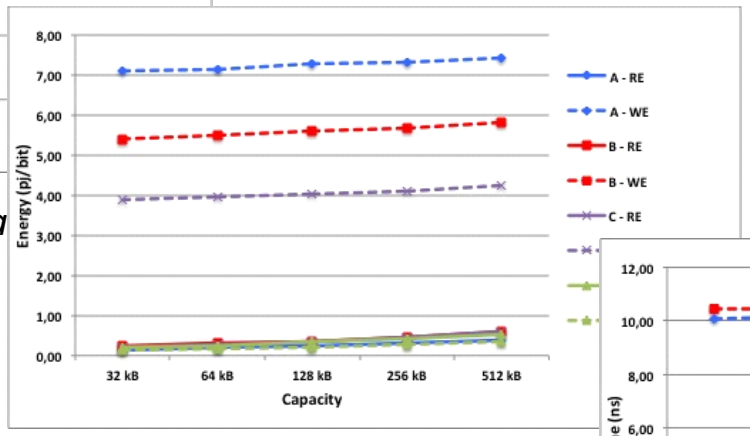
STT-MRAM in CACTI

- High-Performance
  - eight-way set-associative cache memories
  - no error correction mechanism
  - array size from 32 kB to 512 kB.
  - each cache has 64 b IN/OUT data interface with a single read-write port.

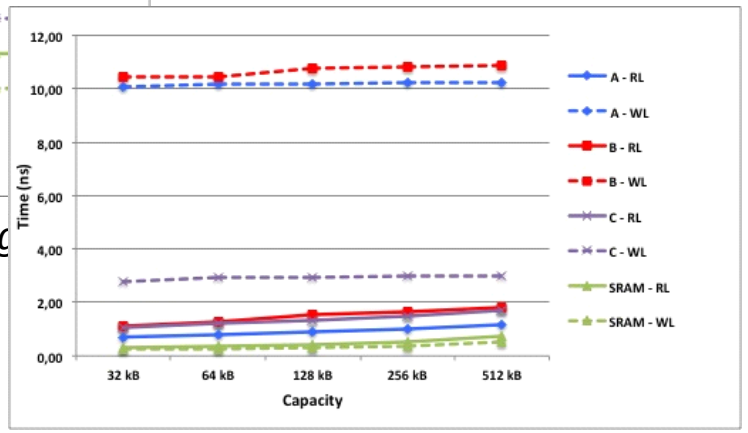
STT-MRAM in CACTI



High Performance - Area

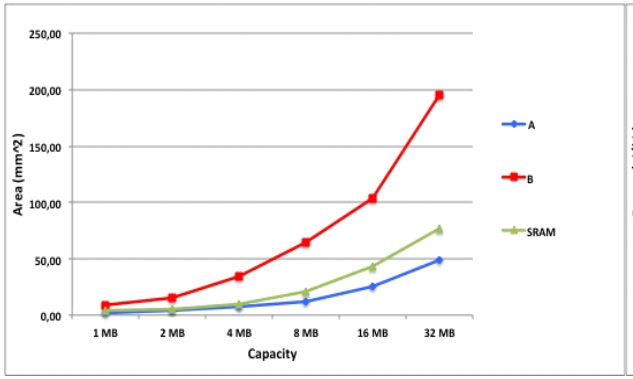


High Performance - Energ

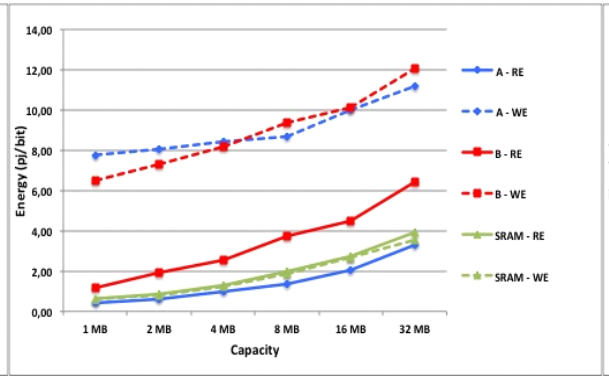


High Performance - Latency

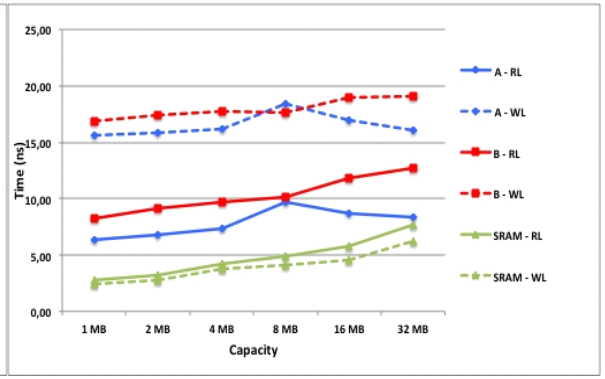
STT-MRAM in CACTI



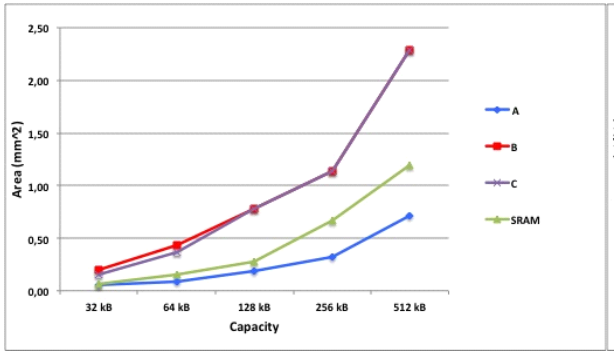
(a) Low Power- Area



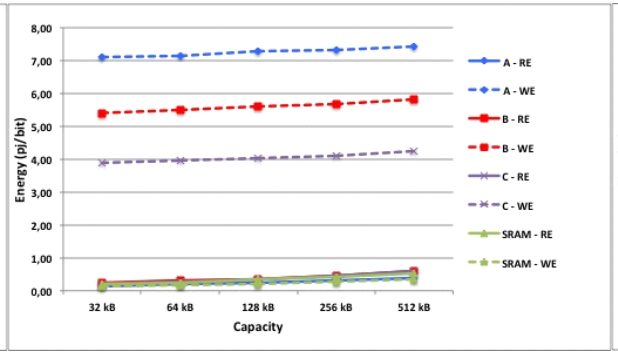
(b) Low Power- Energy



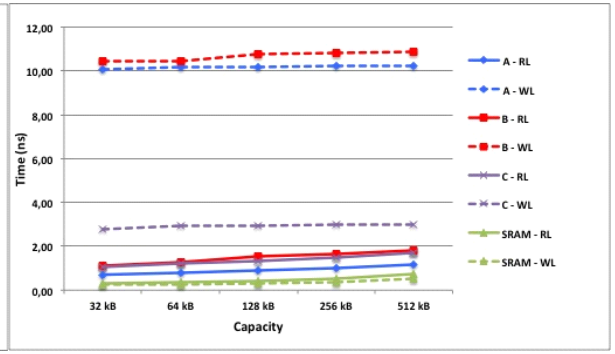
(c) Low Power- Latency



(d) High Performance- Area



(e) High Performance- Energy



(f) High Performance- Latency

High-Performances and Low-Power cache memory designs

STT-MRAM in CACTI

- Preliminary work based on:
  - first order STT-MRAM modeling
  - In-plane STT-MTJ structure
  - Nominal Process parameters
- Future work
  - Complex STT-MRAM model
  - Include perpendicular STT-MTJ structure
  - Include process variability effects