Power-Aware Voltage Tuning for STT-MRAM Reliability

Elena I. Vatajelu, R. Rodriguez-Montañés, S. Di Carlo, M. Indaco, M. Renovell, P. Prinetto, J. Figueras

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ETS

Memories Today

	SRAM	DRAM	Flash
Cell Size	$120F^2$	4-6F	$4\text{-}5\ F^2$
Read Access Time	<1ns	20ns	25,000ns
Write1 Access Time	<1n	0ns	200,000ns
Write0 Access Time	<1ns	20ns	200,000ns
Endurance	>10	10^{15}	10^4
Non-volatility	NO	NO	

Outline

- Introduction to STT-MRAM cell
- STT-MRAM cell operation principle
- STT-MRAM parametric reliability analysis
  - Failure mechanisms
  - Control voltage influence on memory cell operation
- STT-MRAM cell reliability estimation
- Conclusions

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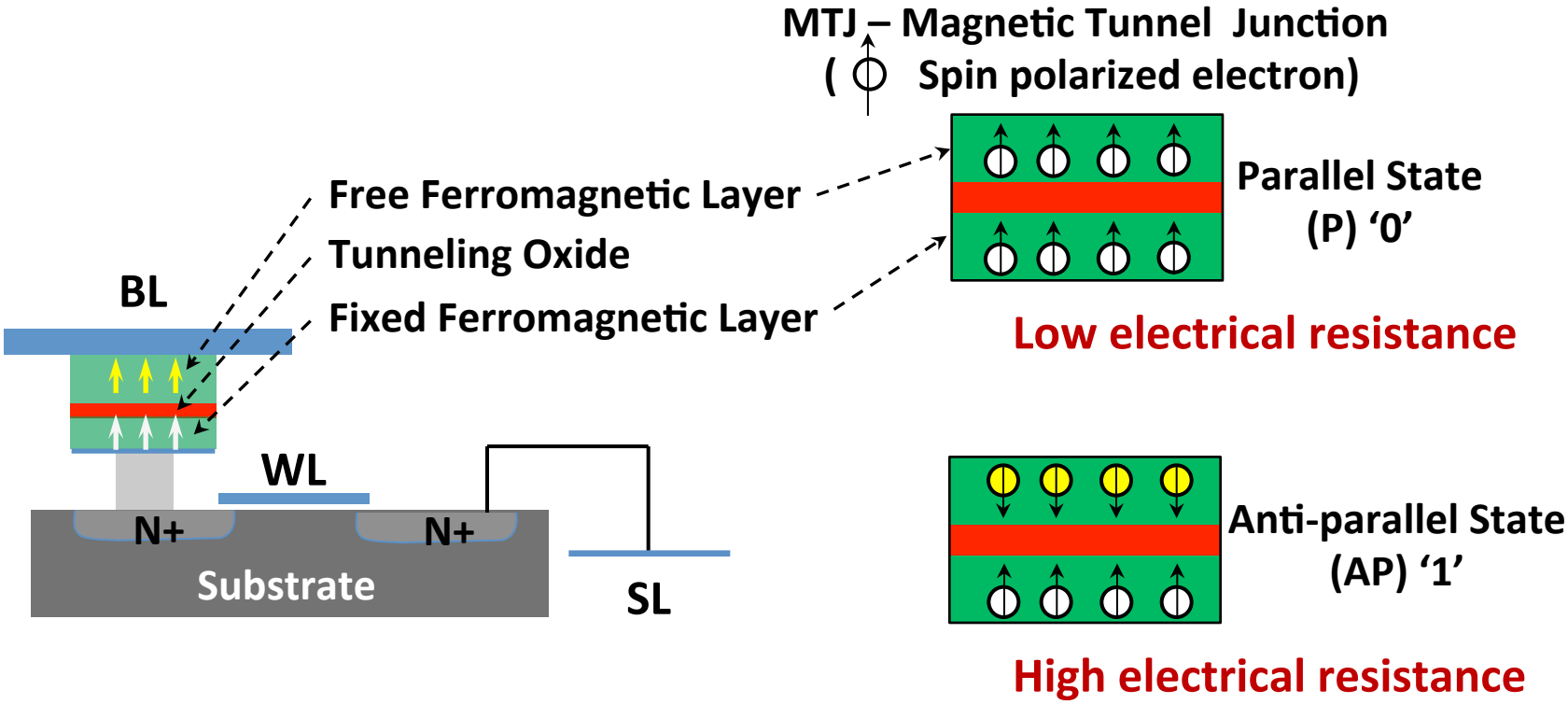
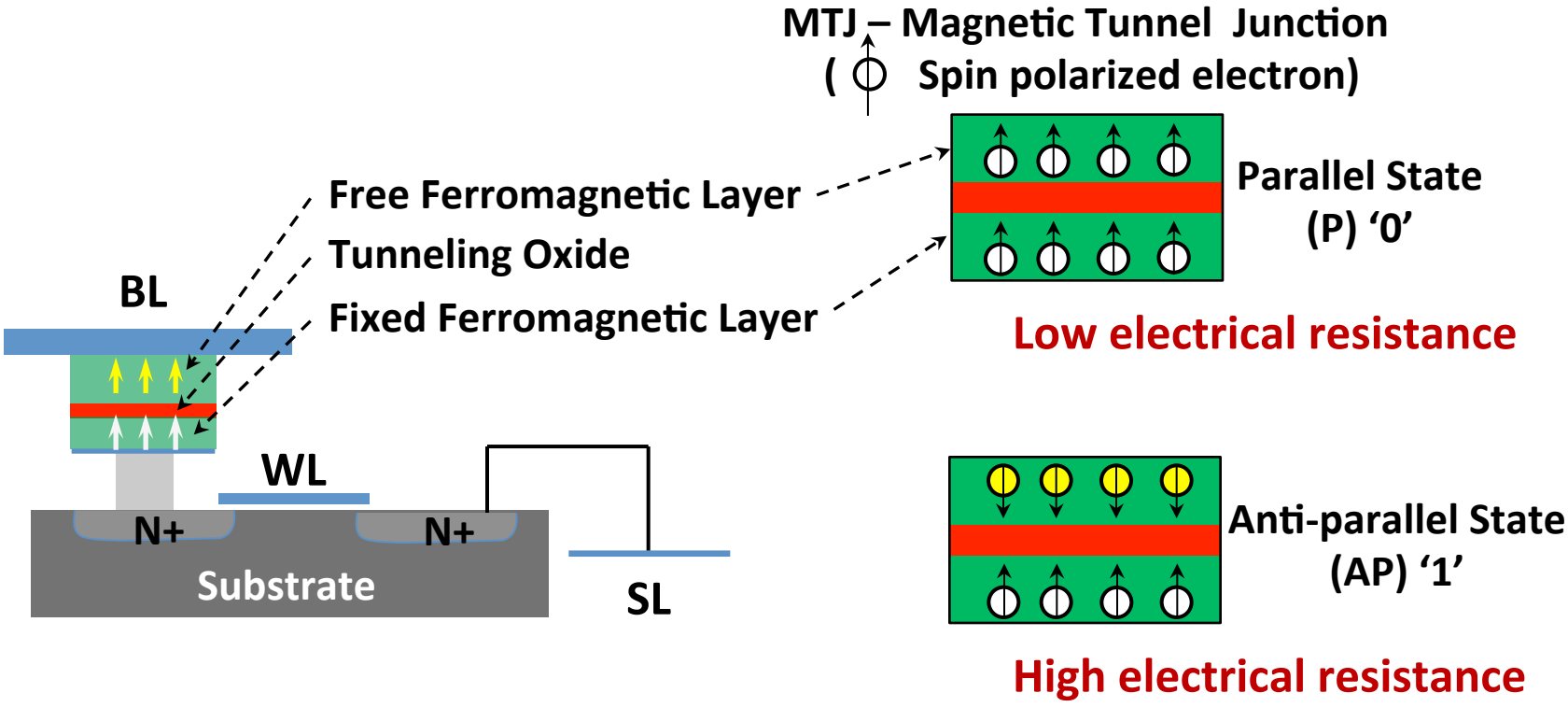
1T1MTJ STT-MRAM Cell



The orientation of the free layer:

- **determines the *resistance* of the material**
- **can be changed by injecting *current*.**

1T1MTJ STT-MRAM Cell



Main resiliency issues come from variations in:

- **Tunneling oxide thickness and cross-section area**
- **Free layer thickness**

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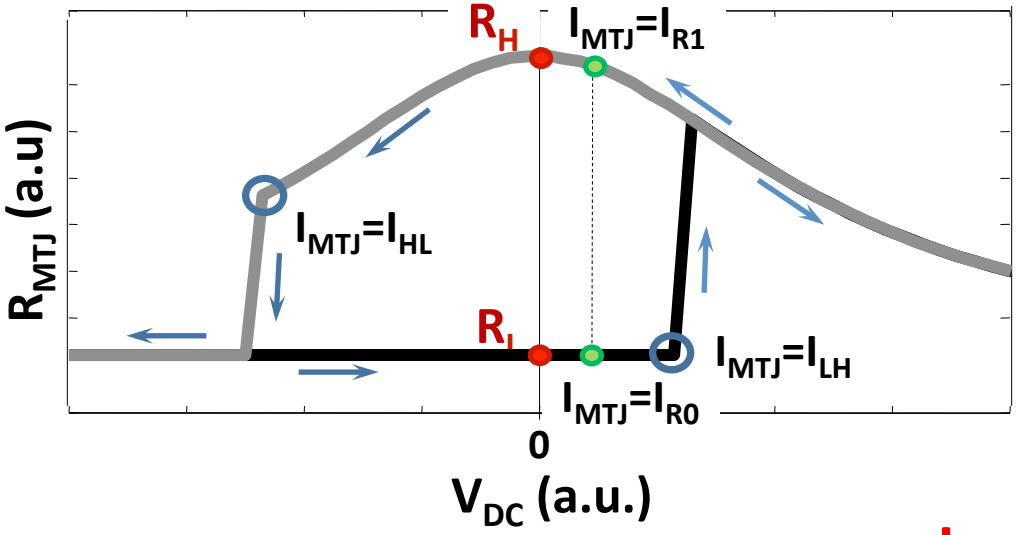
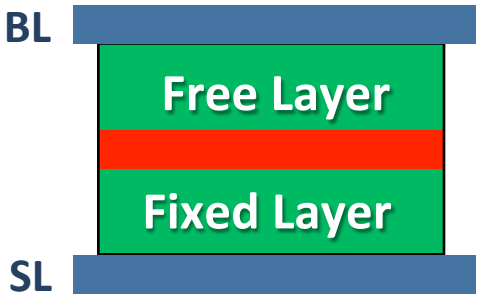
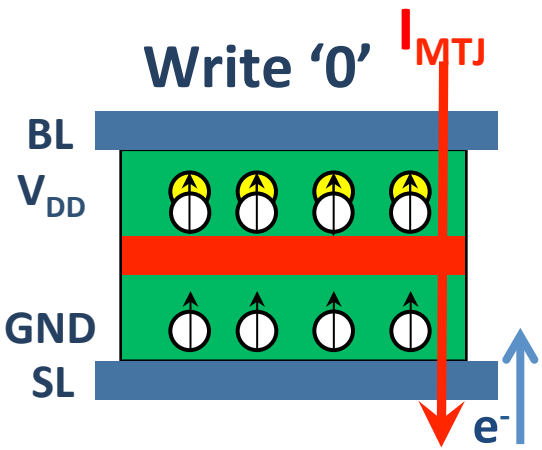
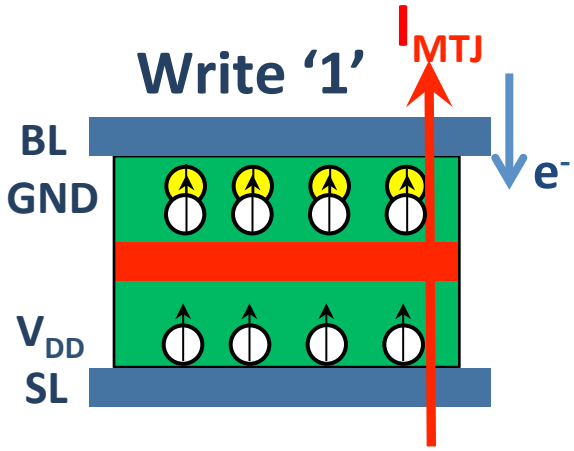
1T1MTJ STT-MRAM Cell

I_{HL} –high to low transition
I_{LH} –low to high transition









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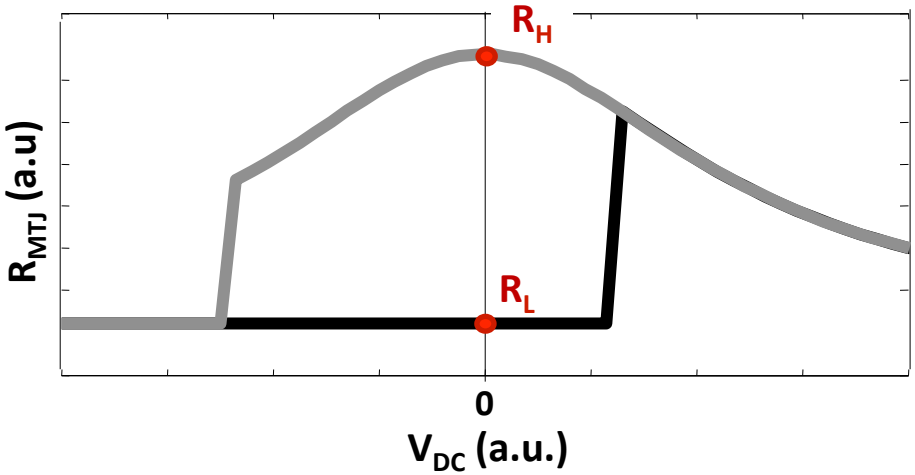
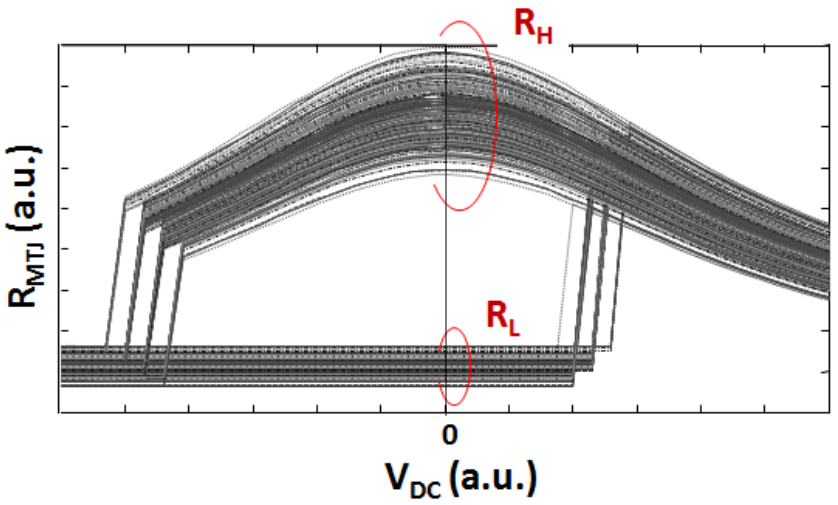
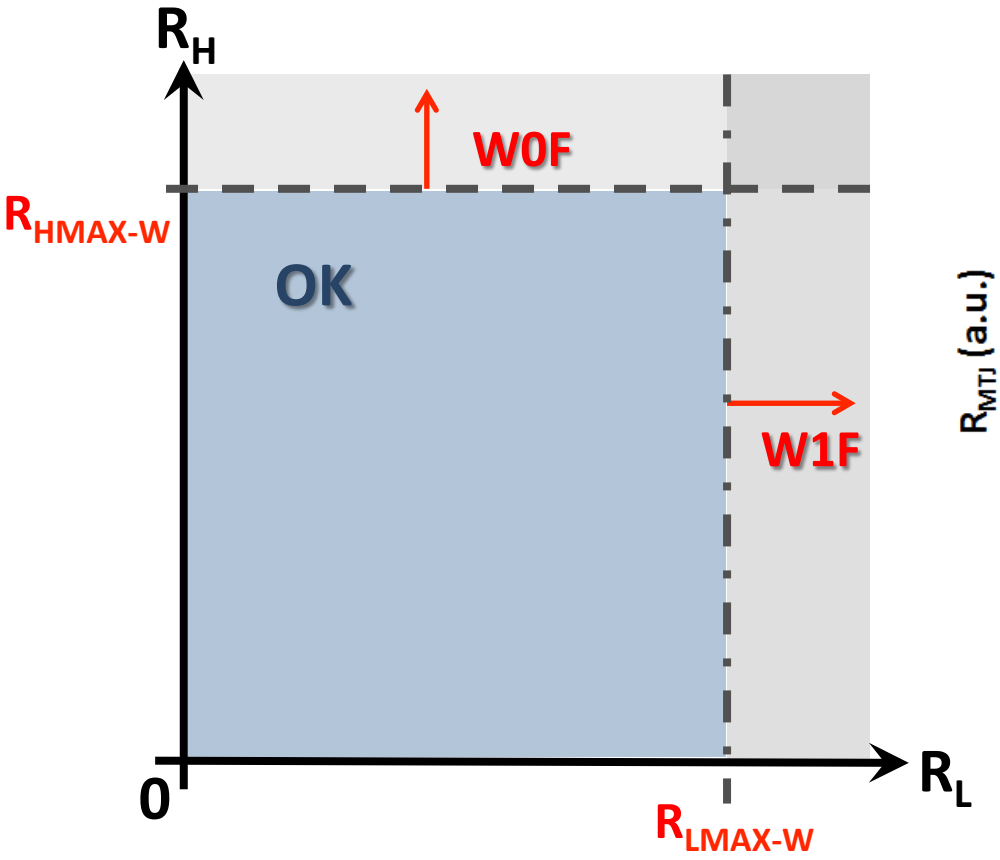
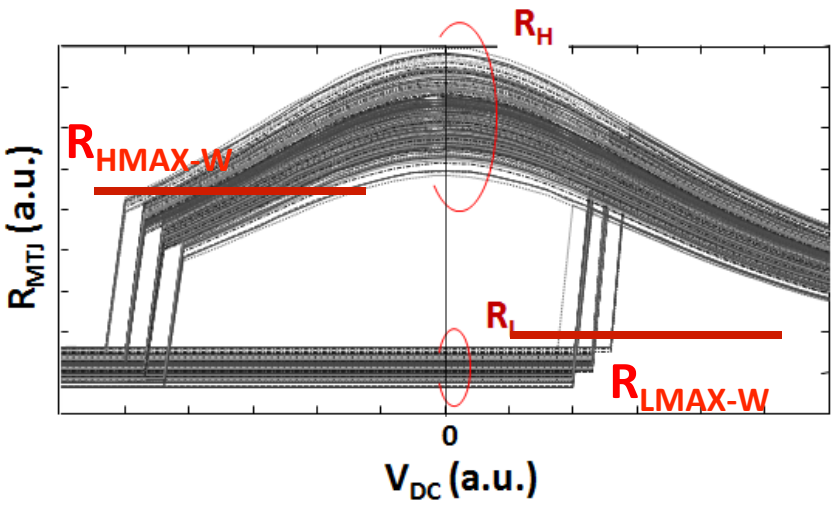
STT-MRAM Failure Mechanisms



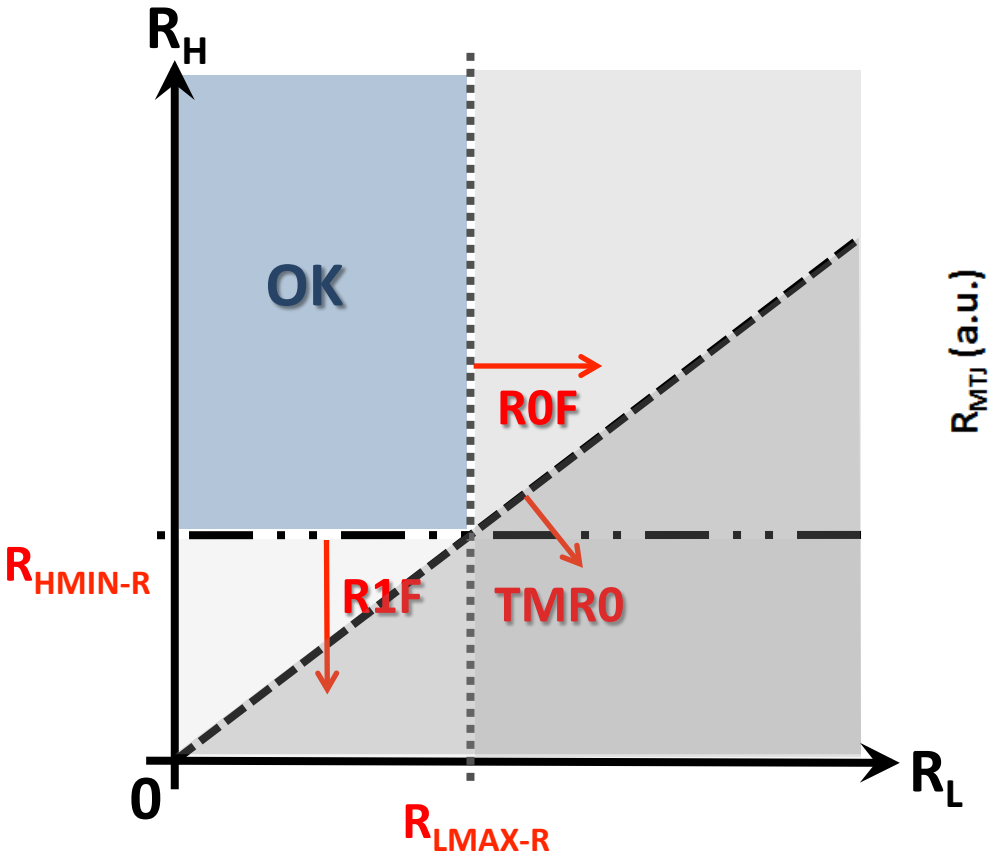


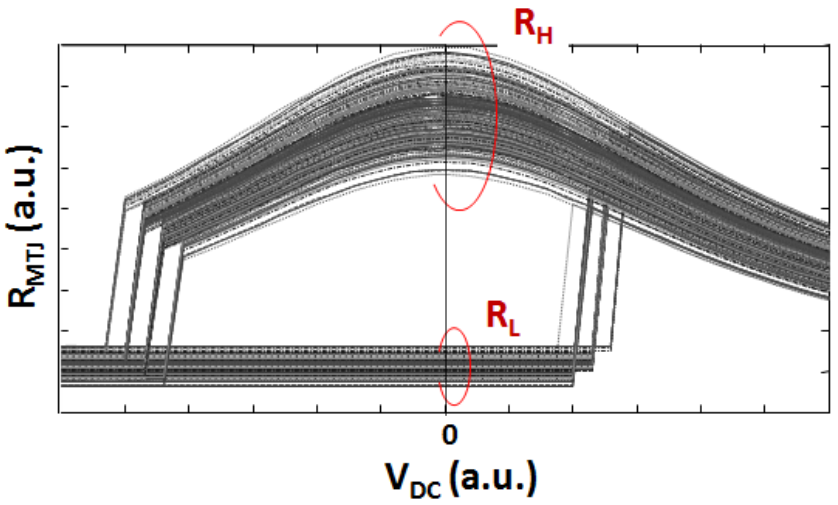
STT-MRAM Failure Mechanisms





STT-MRAM Failure Mechanisms





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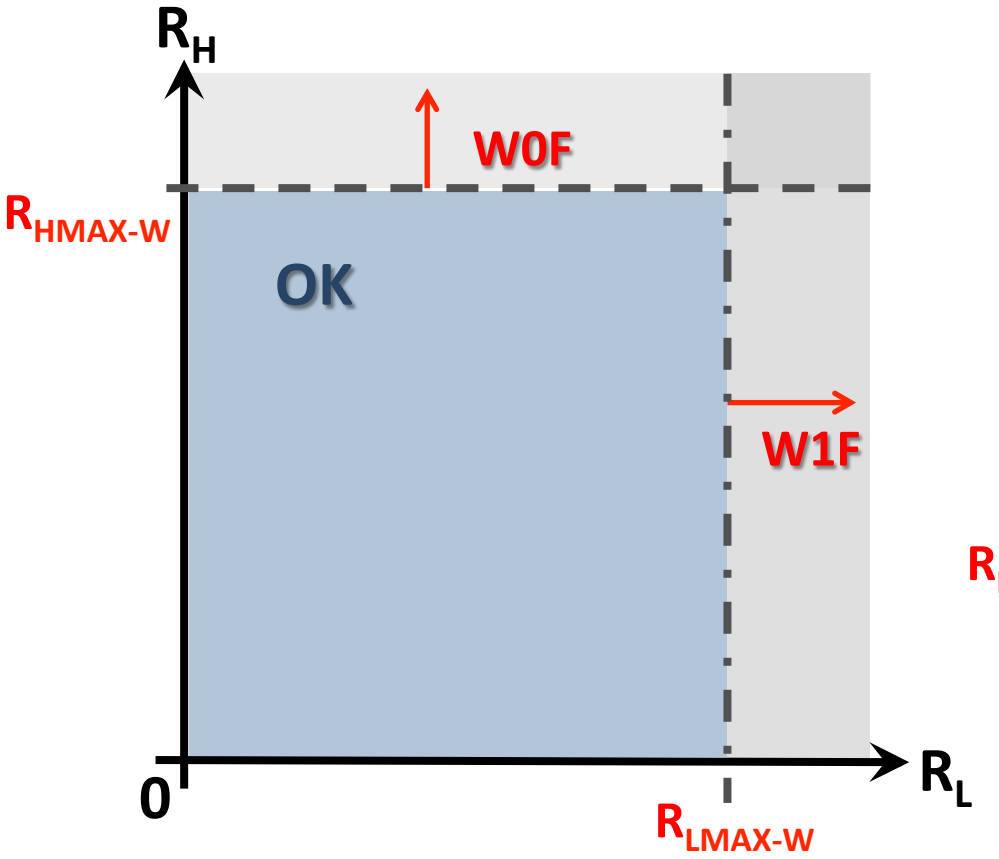

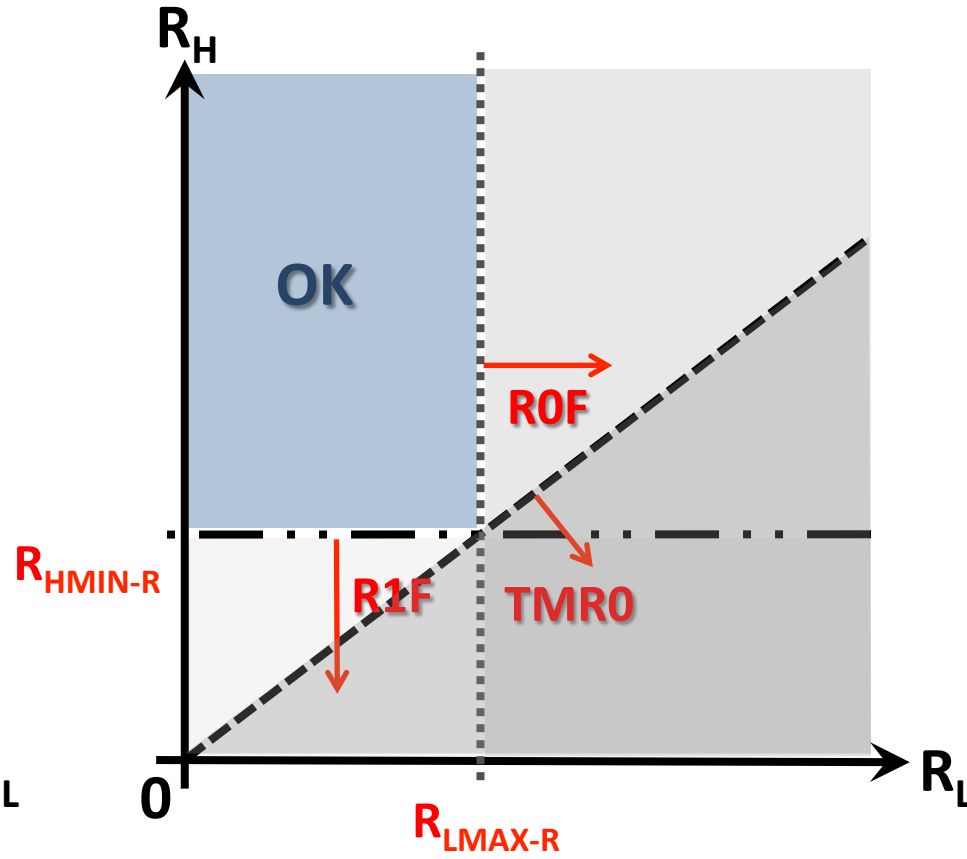

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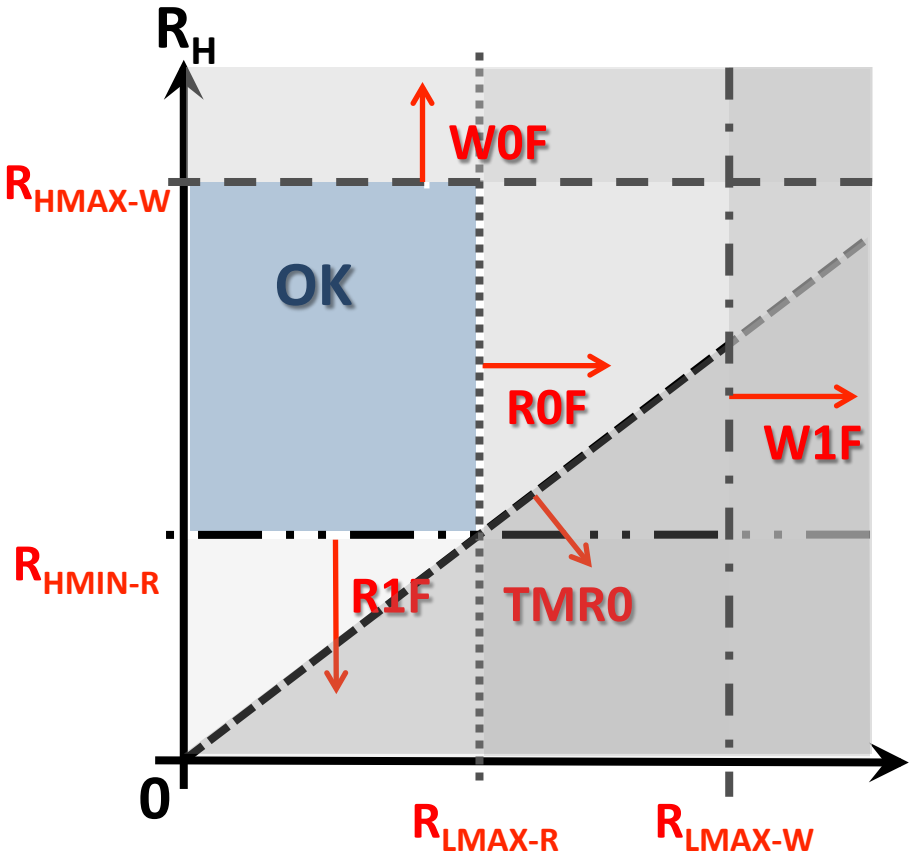
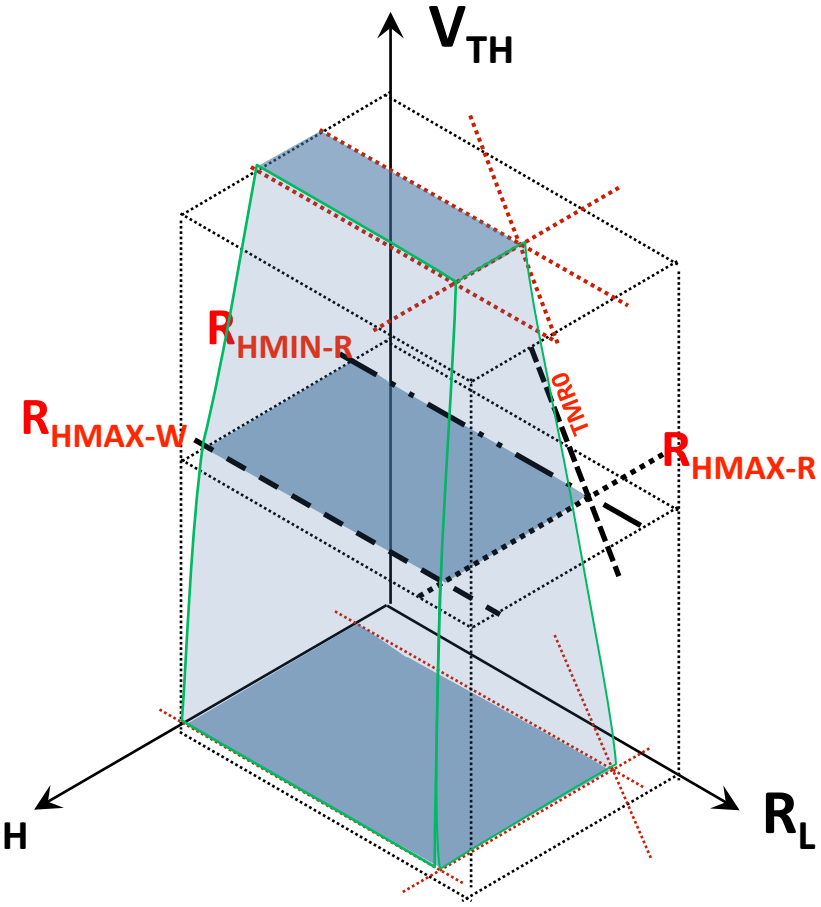




$$P_{RF\&WF} = 1 - \int_{0}^{\min(R_{LMXAX-R}, R_{LMXAX-W})} \int_{R_{HMIN-R}}^{R_{HMAX-W}} \int_{V_{TH-\min}}^{V_{TH-\max}} f(R_L, R_H, V_{TH}) dR_L dR_H dV_{TH}$$

STT-MRAM Failure Mechanisms

- Magnetic nanostructures suffer from thermally activated magnetization reversal.
- Néel-Brown: at finite temperature, there is a finite probability for the magnetization to flip and reverse its direction.
- Néel-Brown model:

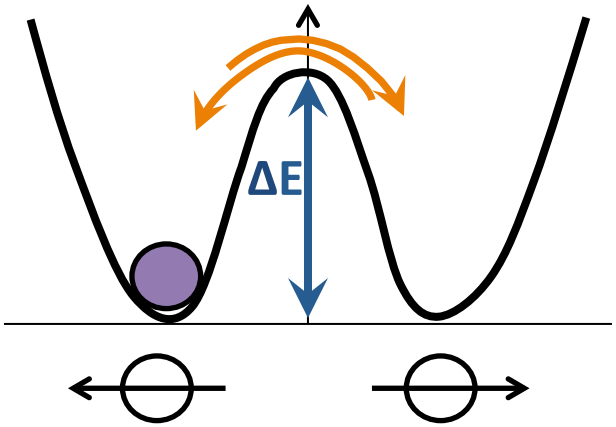
$$P(t) = exp(t/\tau)$$

$$\tau = \tau_0 \, exp(\Delta E / k_B T)$$

STT-MRAM Failure Mechanisms

- **STT-MRAM Cell Failure Probability in Data Retention:**

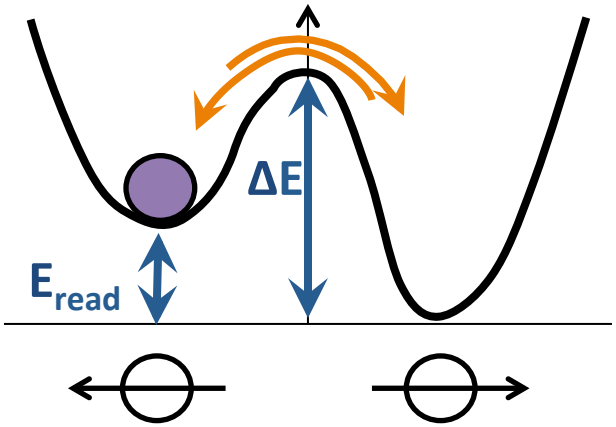
$$P(t) = 1 - exp[(-Nt/\tau_0)\cdot exp(-\Delta E/k_B T)]$$



STT-MRAM Failure Mechanisms

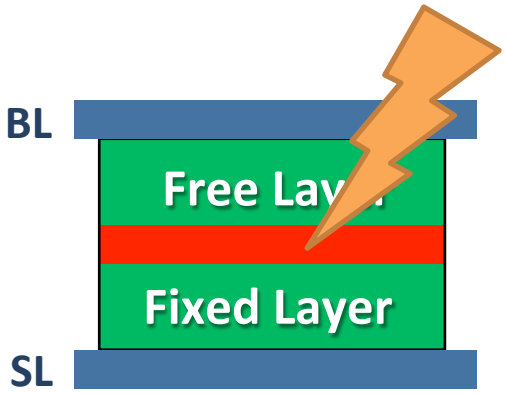
- **STT-MRAM Cell Failure Probability in Read Operation**

$$P(t) = 1 - exp[(-Nt/\tau_0)\cdot exp(-\Delta E(1 - (I_{read}/I_{0C}))/k_BT)]$$



STT-MRAM Failure Mechanisms

- ***Aging:*** **STT-MRAM Cell Failure due to Tunneling Oxide Breakdown**



R_H degradation due to Tunneling Oxide stress:

$$R_H(t) = \frac{R_H(0)}{1 + F(t)\left[R_H(0)/R_H(t_{BD}) - 1\right]}$$

with F(t) following a Weibull distribution:

$$F(t) = 1 - exp\left(-(t/\lambda)^k\right)$$

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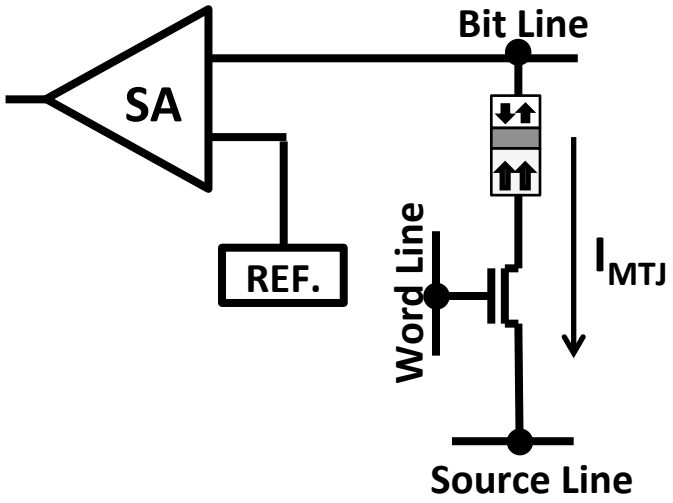
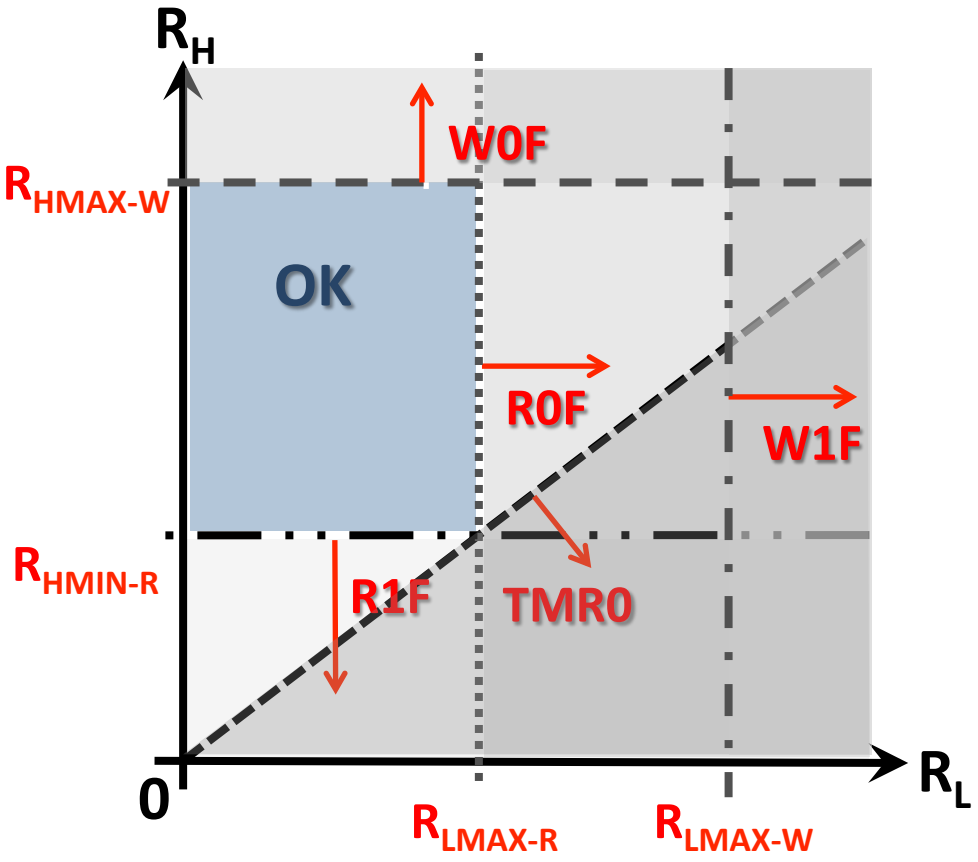
Control voltage effect on STT MRAM cell operation



Knobs
- V_{DD}
- V_{WL}
- V_{BL-SL}



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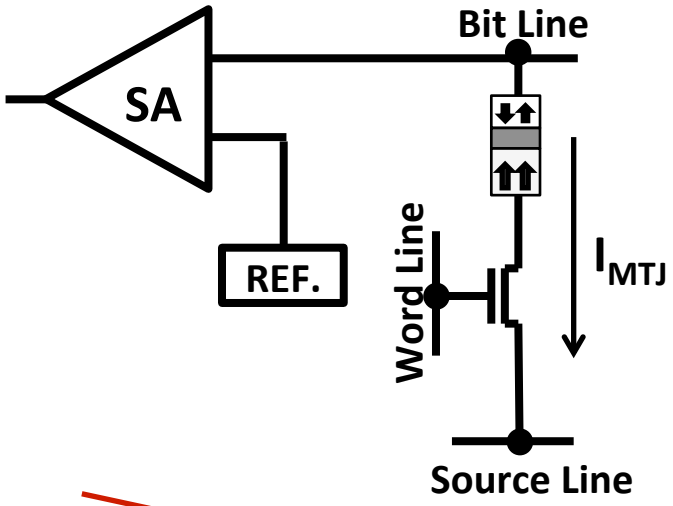

Knobs
- V_{DD}
- V_{WL}
- V_{BL-SL}

$$P(t) = 1 - exp[(-Nt/\tau_0)\cdot exp(-\Delta E/k_B T)]$$

$$P(t) = 1 - exp[(-Nt/\tau_0)\cdot exp(-\Delta E(1 - (I_{read}/I_{0C}))/k_B T)]$$

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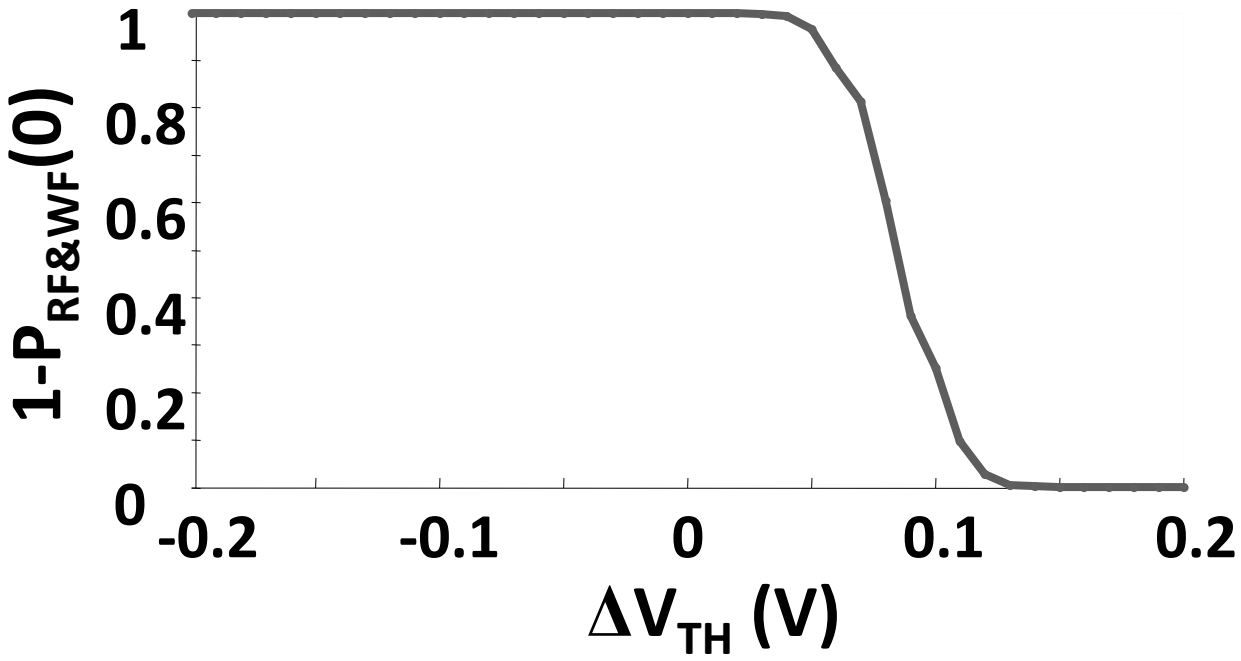
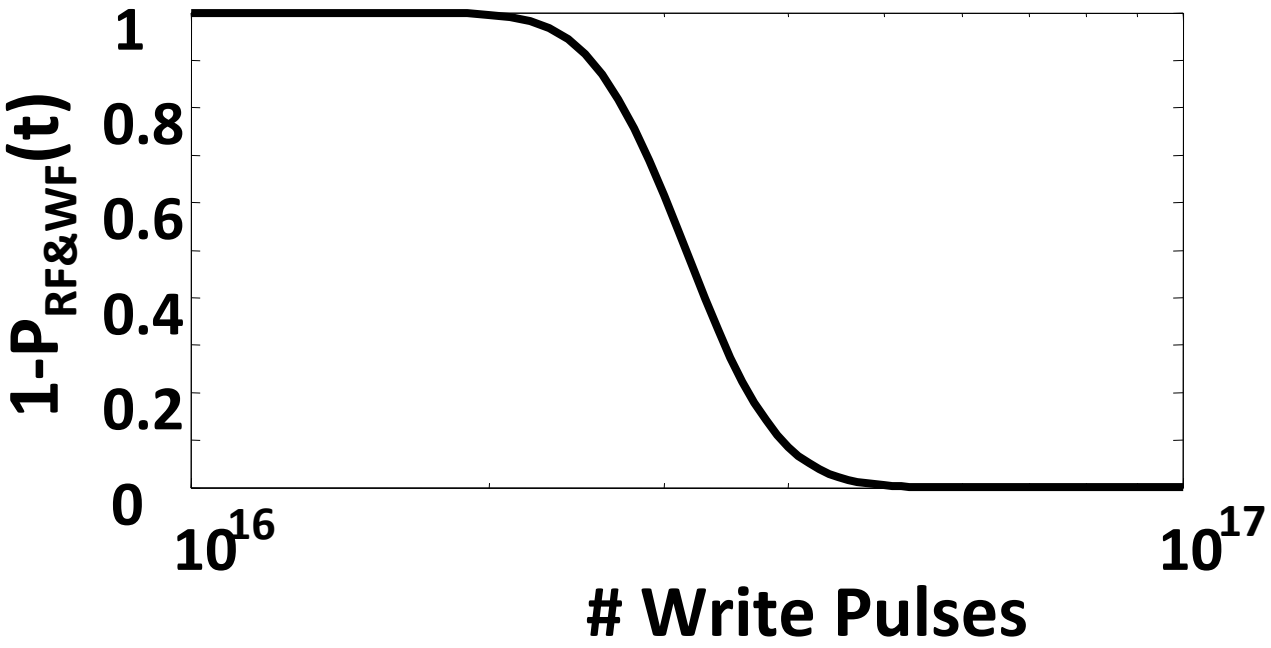
STT-MRAM cell reliability

No knobs, Fresh Cell, 2D analysis with swipe V_{TH}



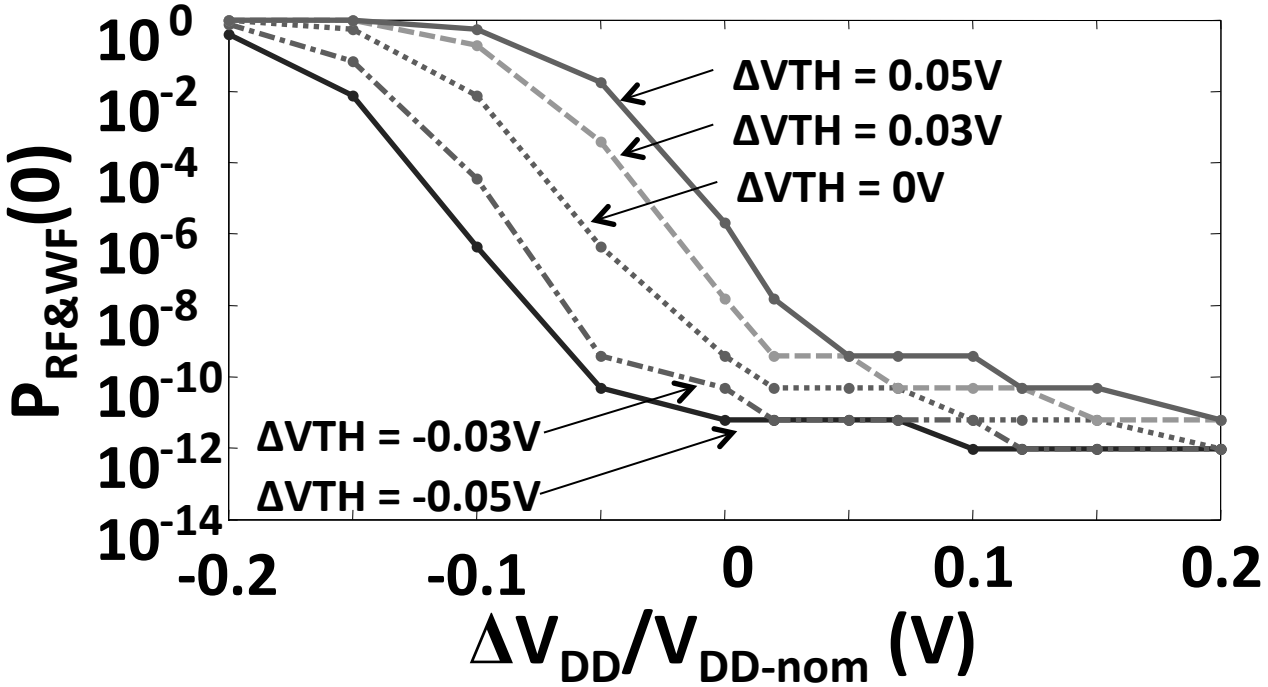
STT-MRAM cell reliability

No knobs, Aged Cell, 3D analysis



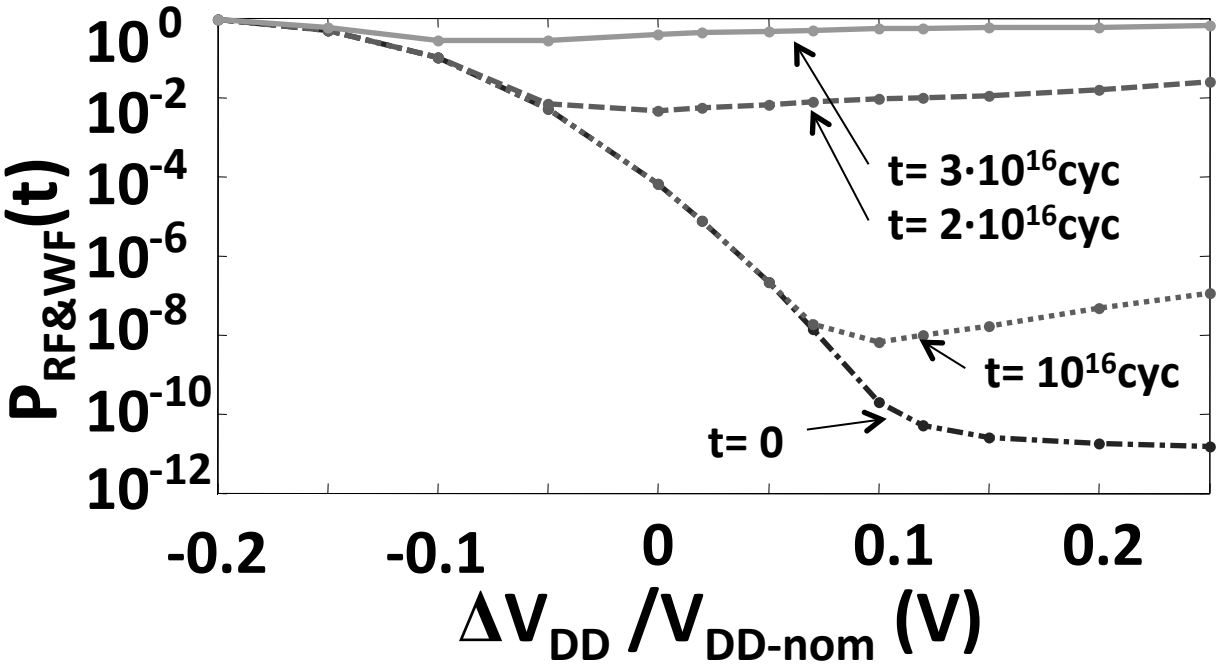
STT-MRAM cell reliability

V_{DD} knob, Fresh Cell, 2D analysis with swipe V_{TH}



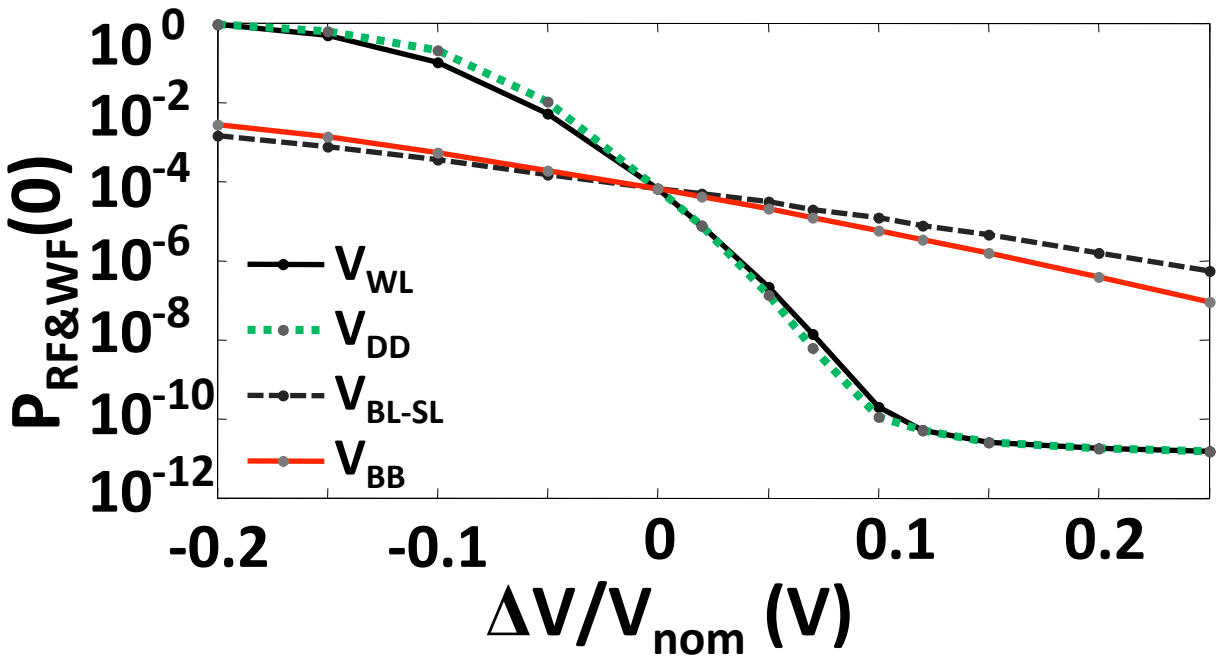
STT-MRAM cell reliability

V_{DD} knob, Aged Cell, 3D analysis



STT-MRAM cell reliability

All knobs, Fresh Cell, 3D analysis



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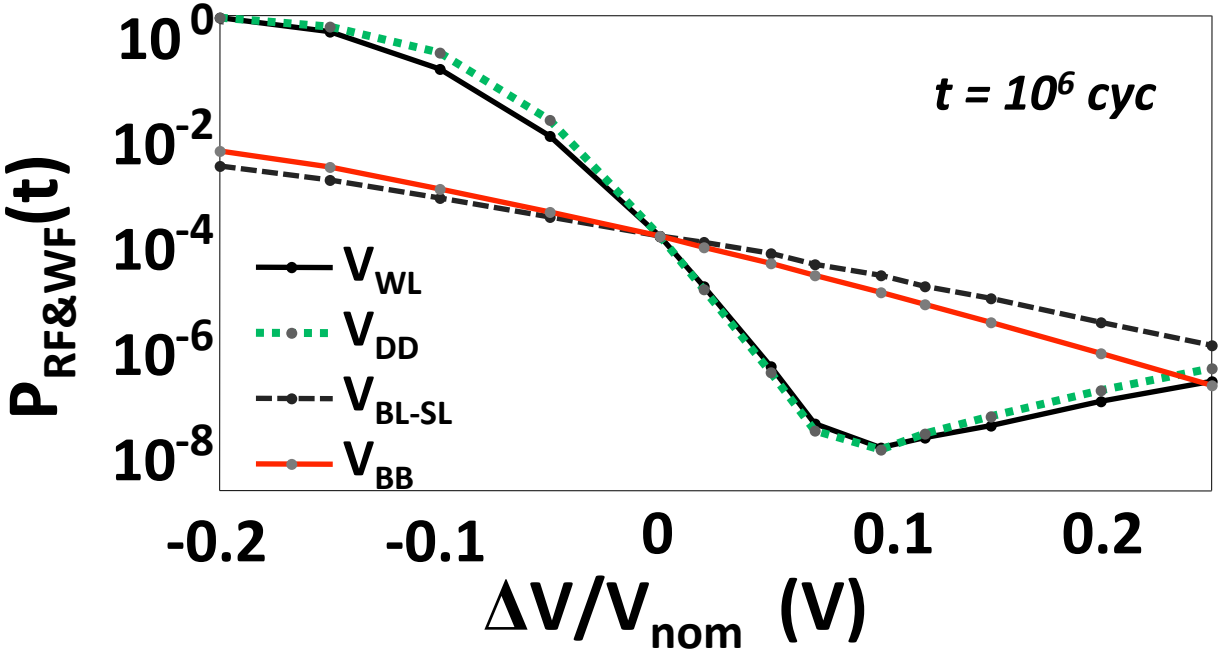
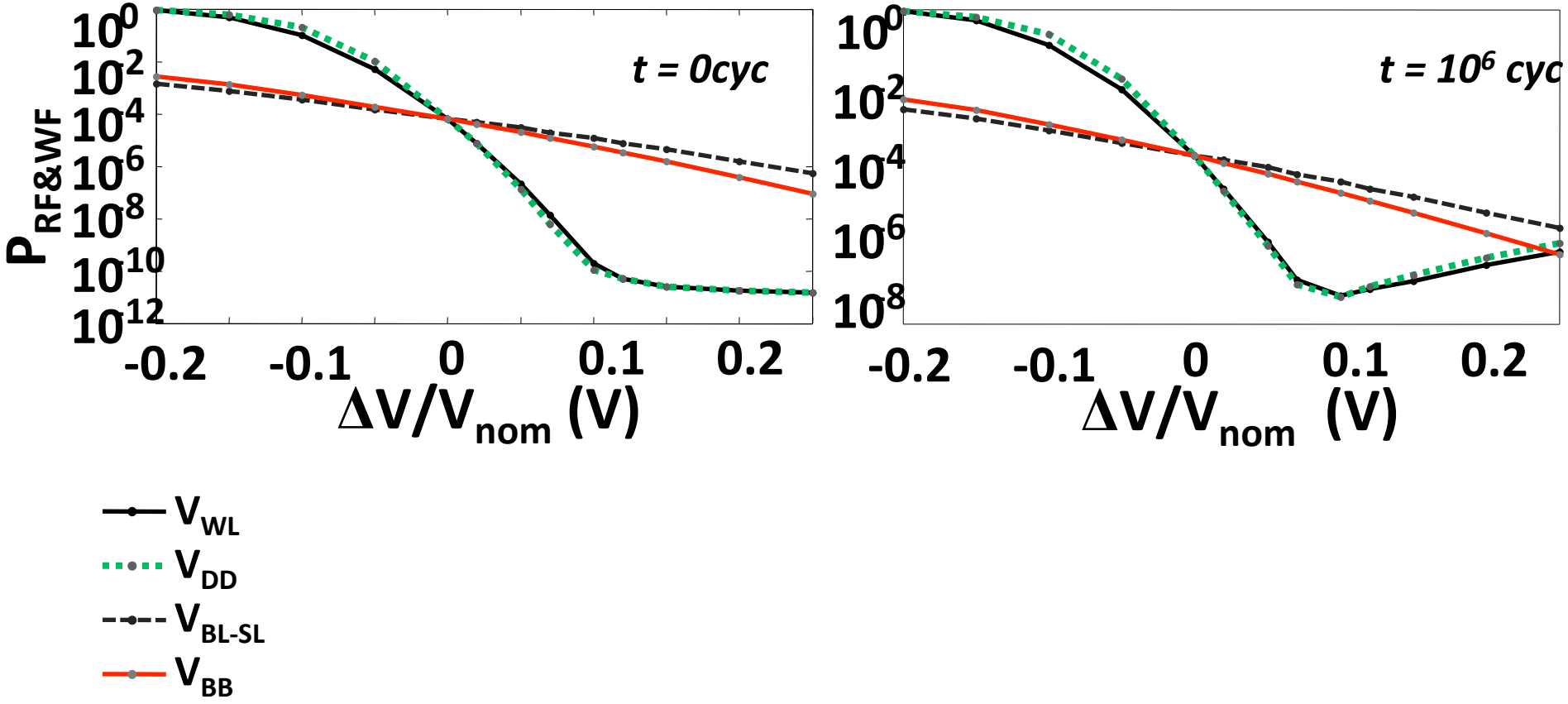
All knobs, Fresh Cell, 3D analysis



STT-MRAM cell reliability

All knobs, 3D analysis



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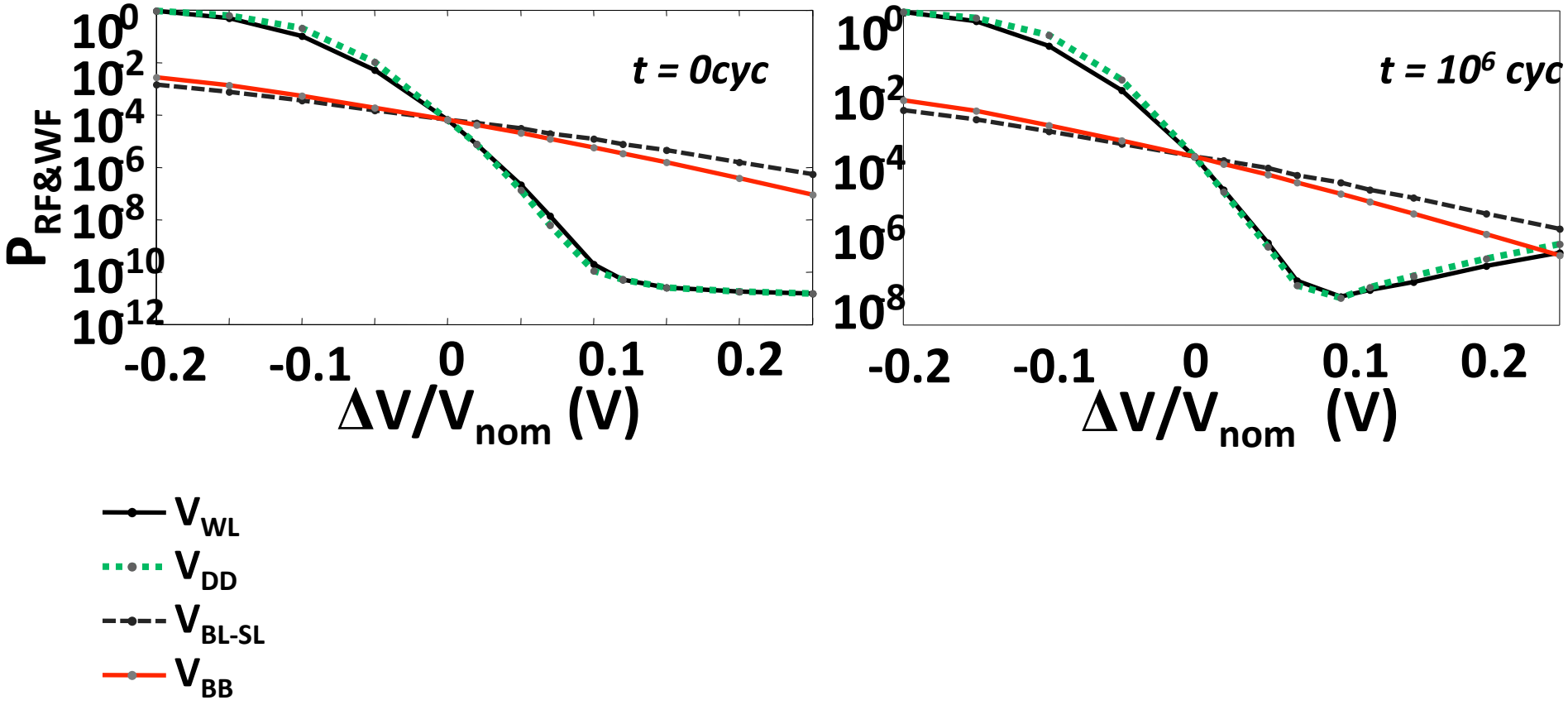
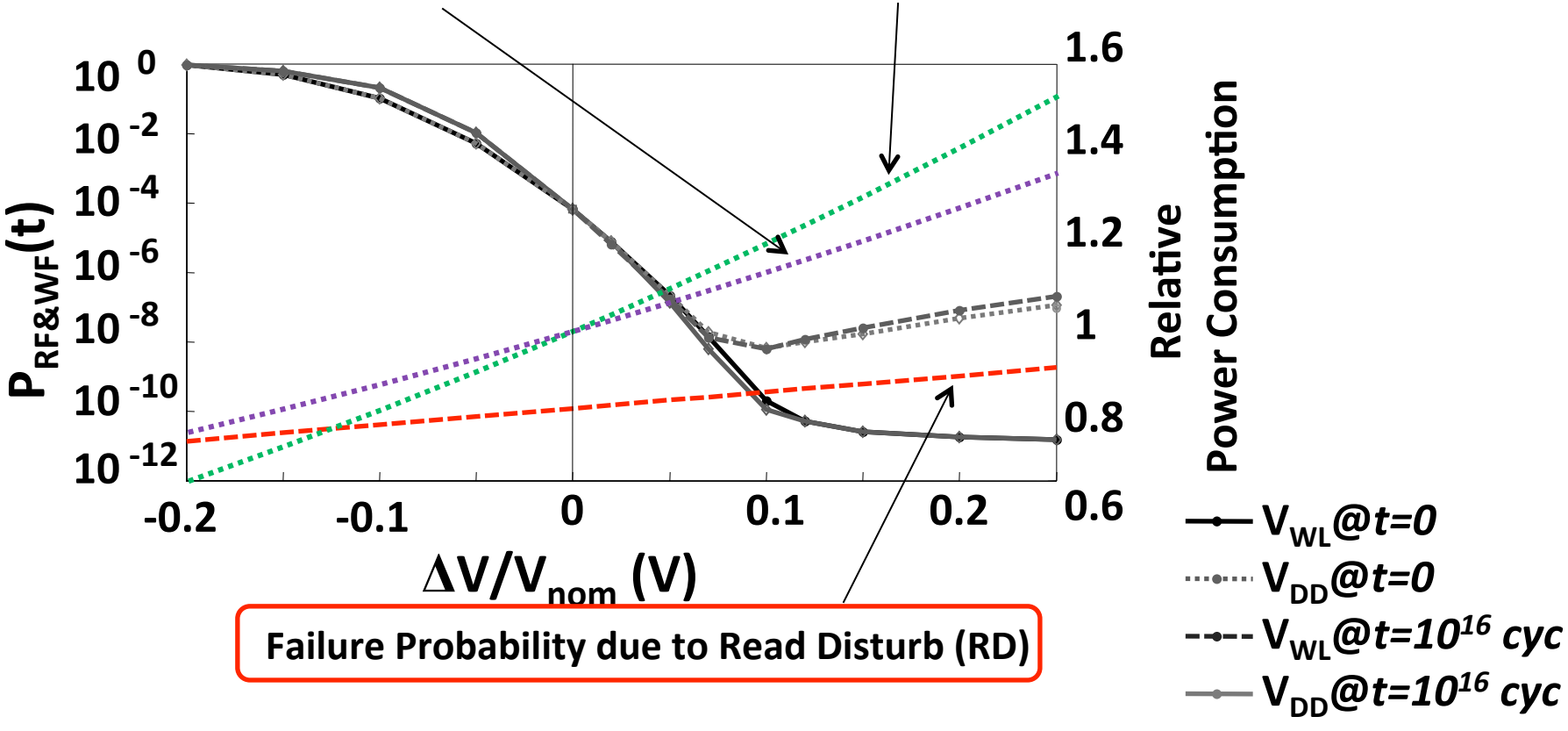


Reliability Power Tradeoff

Power Consumption when varying V_{WL}

Power Consumption when varying V_{DD}



Failure Probability due to Read Disturb (RD)

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Conclusions

- STT-MRAM reliability evaluation methodology
- The joint effect of
  - fabrication- and aging-induced process variability
- Reliability evaluation under voltage tuning
- Power aware reliability estimation to identify optimum voltage value for STT-MRAM operation

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