



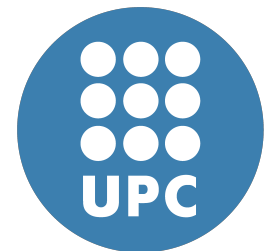
STT-MRAM Cell Reliability Evaluation under Process, Voltage and Temperature (PVT) Variations

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Memories Today

	SRAM	DRAM	Flash
Cell Size	120F ²	4-6F ² 	4-5 F ²
Read Access Time	<1ns 	20ns	25,000ns
Write1 Access Time	<1ns 	20ns	200,000ns
Write0 Access Time	<1ns	20ns	200,000ns
Endurance	>10 ¹⁵ 	10 ¹⁵	10 ⁴
Non-volatility	NO	NO	

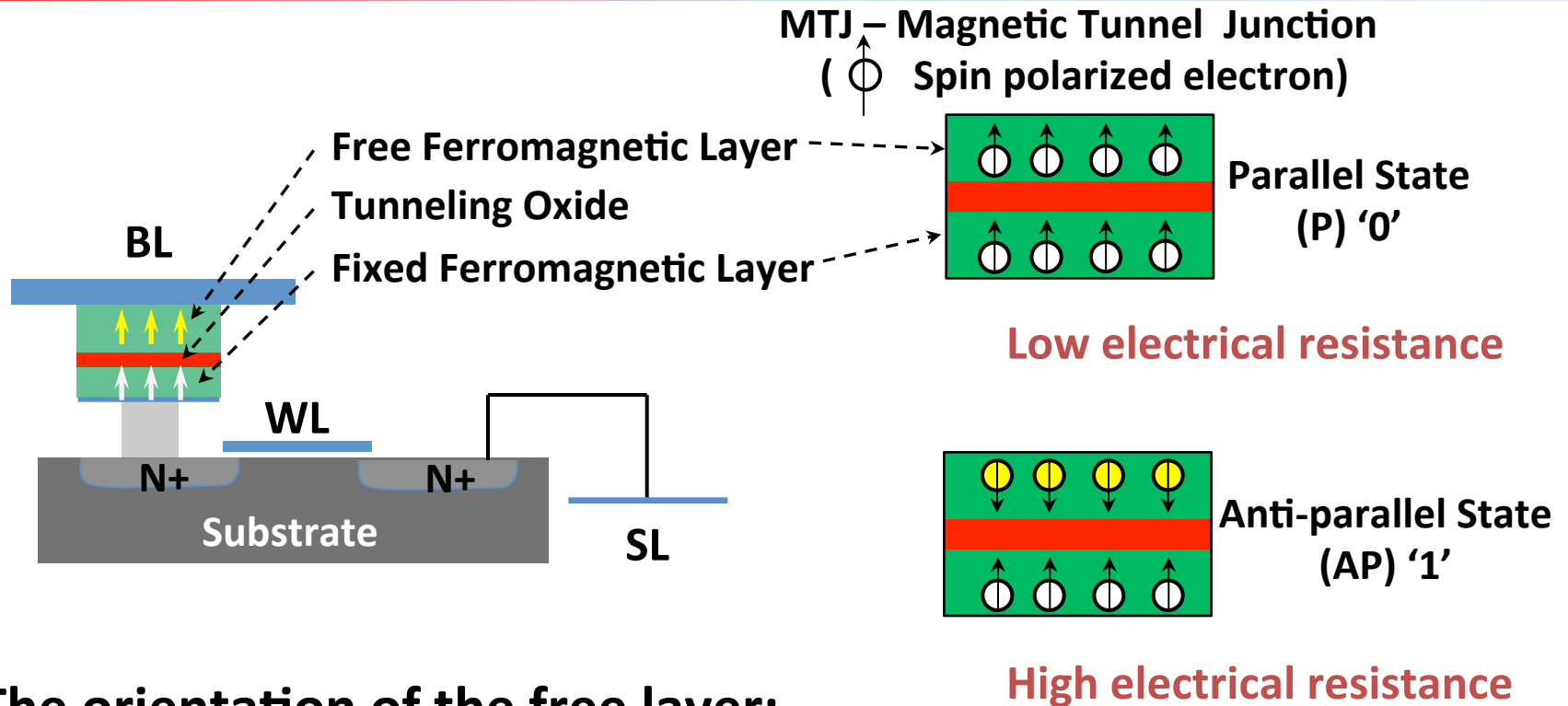
Outline

- Introduction to STT-MRAM cell
- STT-MRAM cell operation principle
- Failure mechanisms of the STT-MRAM cell
- STT-MRAM cell reliability under PVT variations
- Conclusions

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- **Introduction to STT-MRAM cell**
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1T1MTJ STT-MRAM Cell

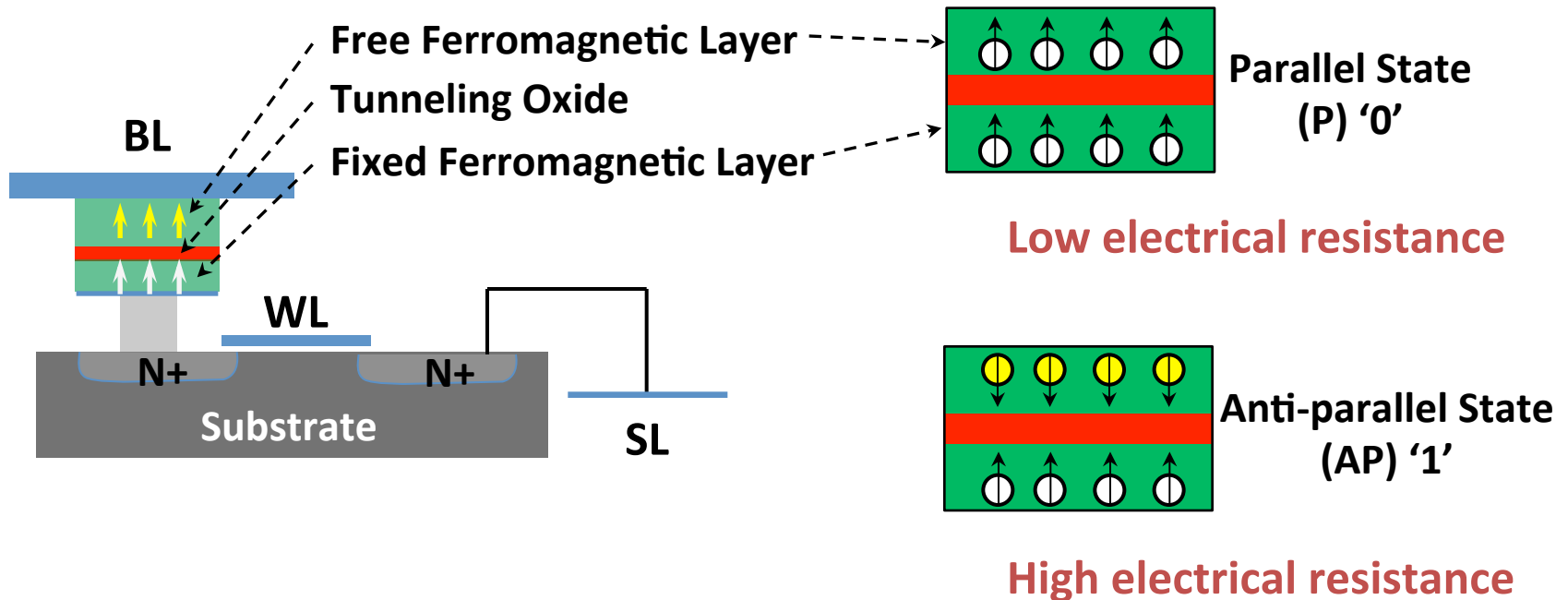


The orientation of the free layer:

- determines the *resistance* of the material
- can be changed by injecting *current*.

1T1MTJ STT-MRAM Cell

MTJ – Magnetic Tunnel Junction
($\ominus \rightarrow$ Spin polarized electron)



Main resiliency issues come from variations in:

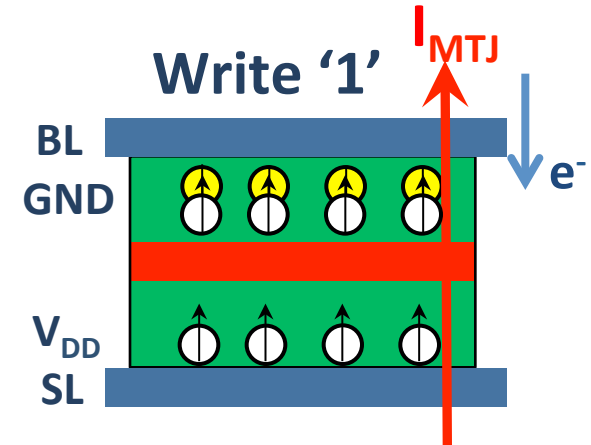
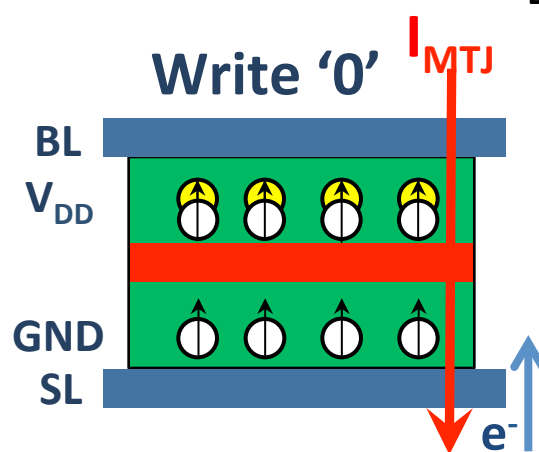
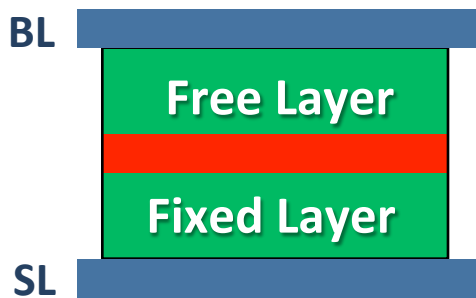
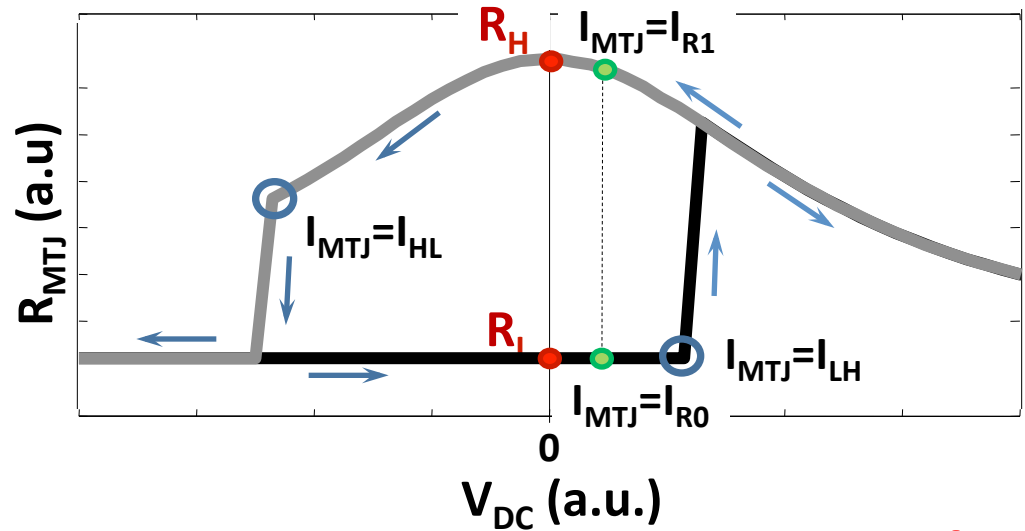
- Tunneling oxide thickness and cross-section area
- Free layer thickness

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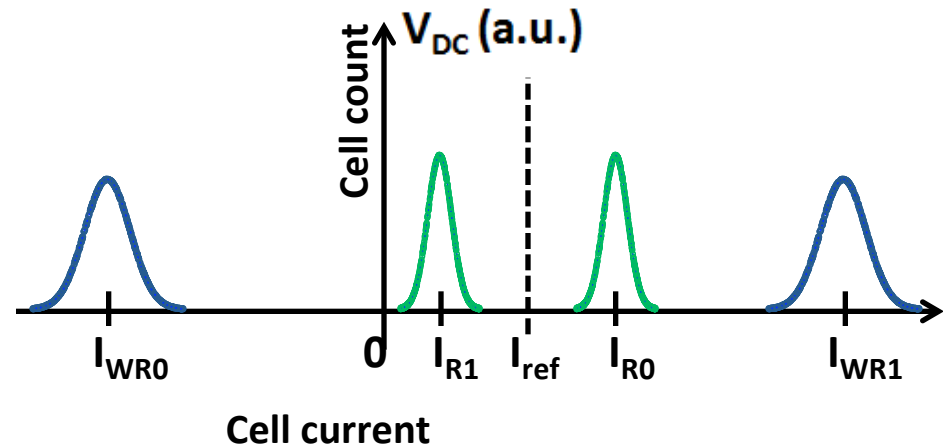
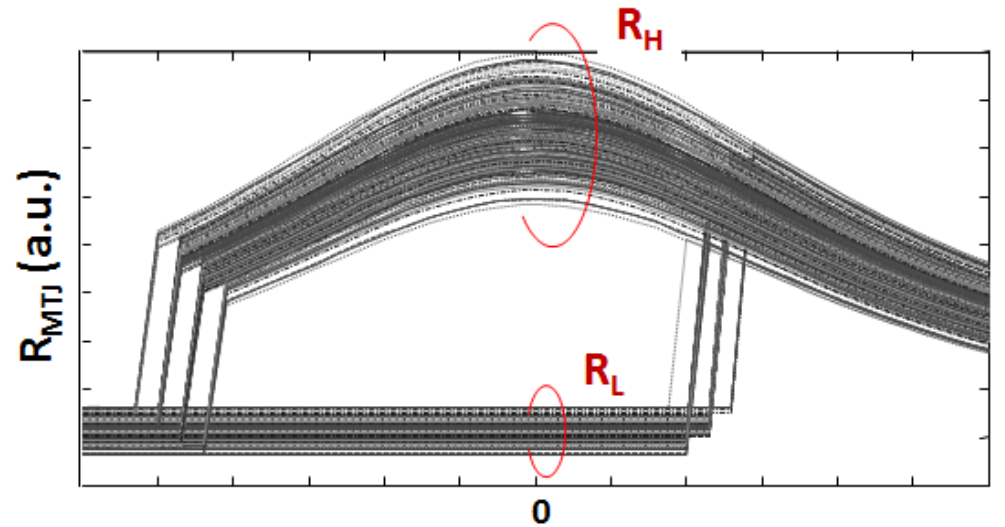
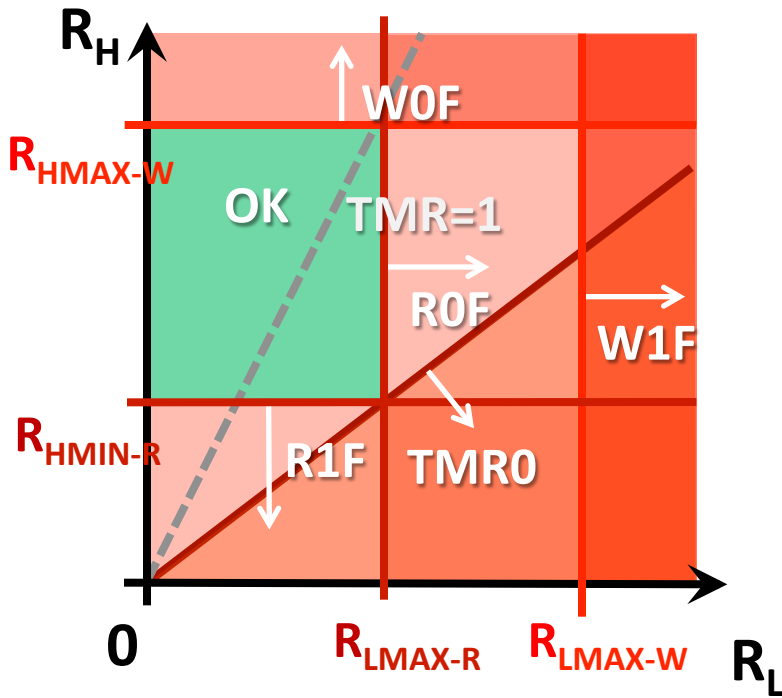
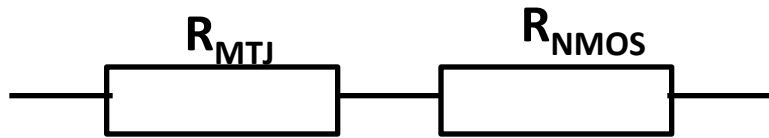
I_{HL} – high to low transition
 I_{LH} – low to high transition



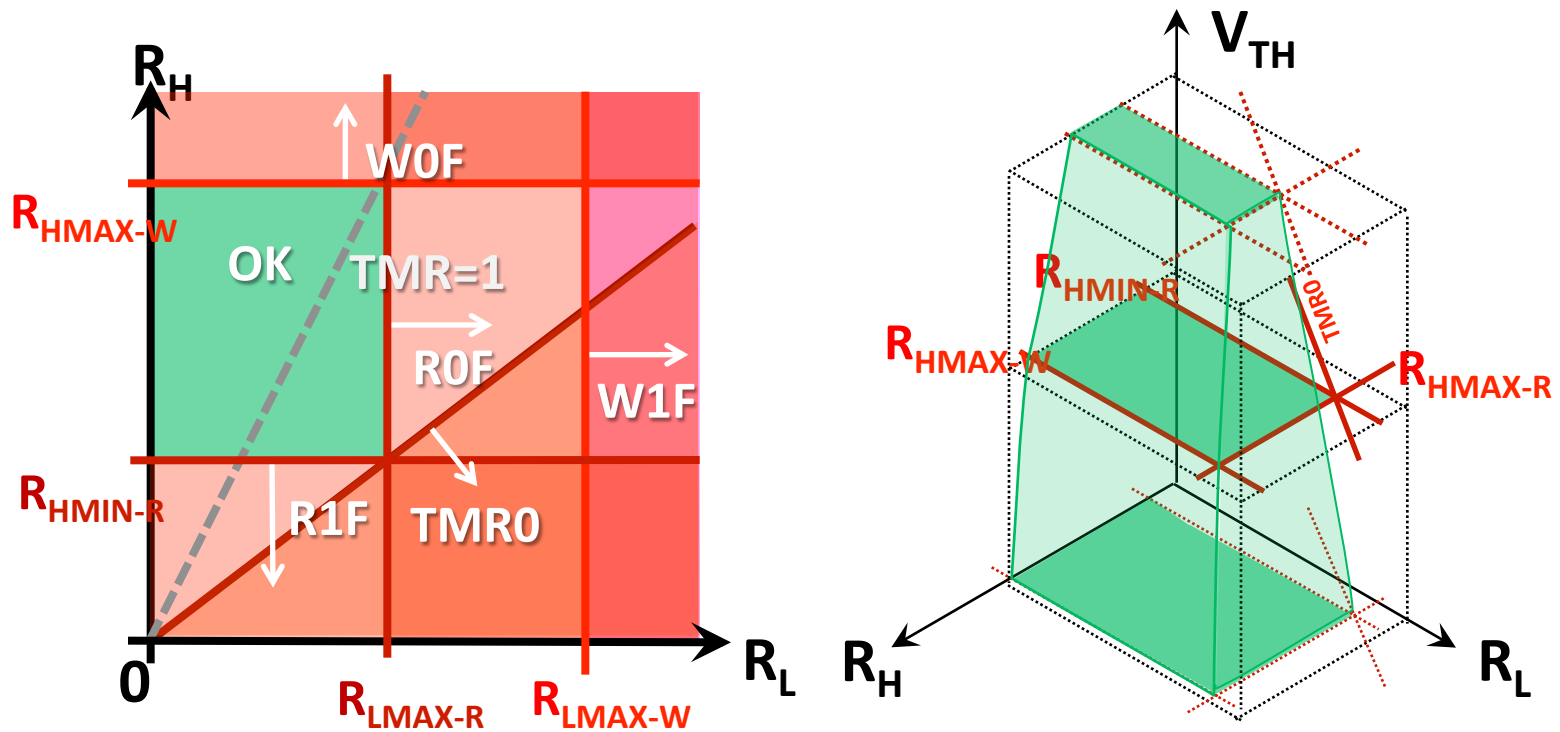
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STT MRAM Cell Failure Mechanisms

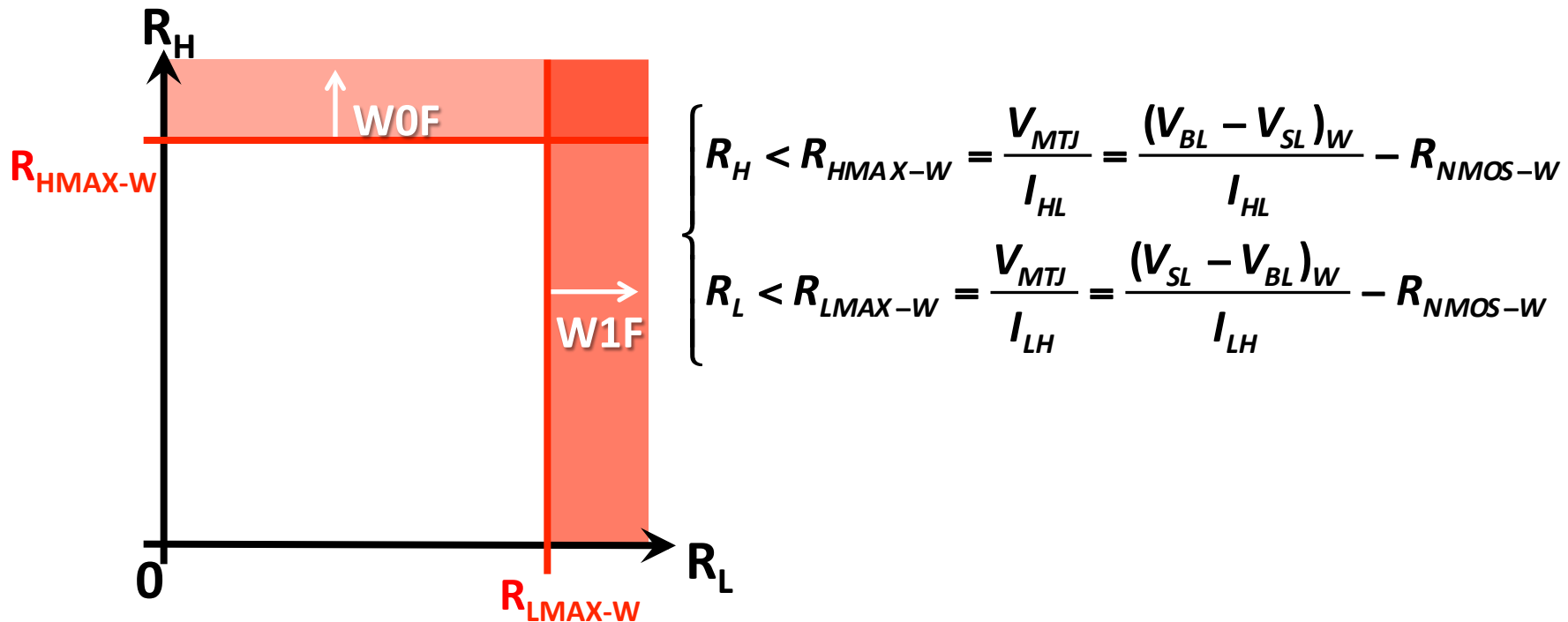


STT MRAM Cell Failure Mechanisms



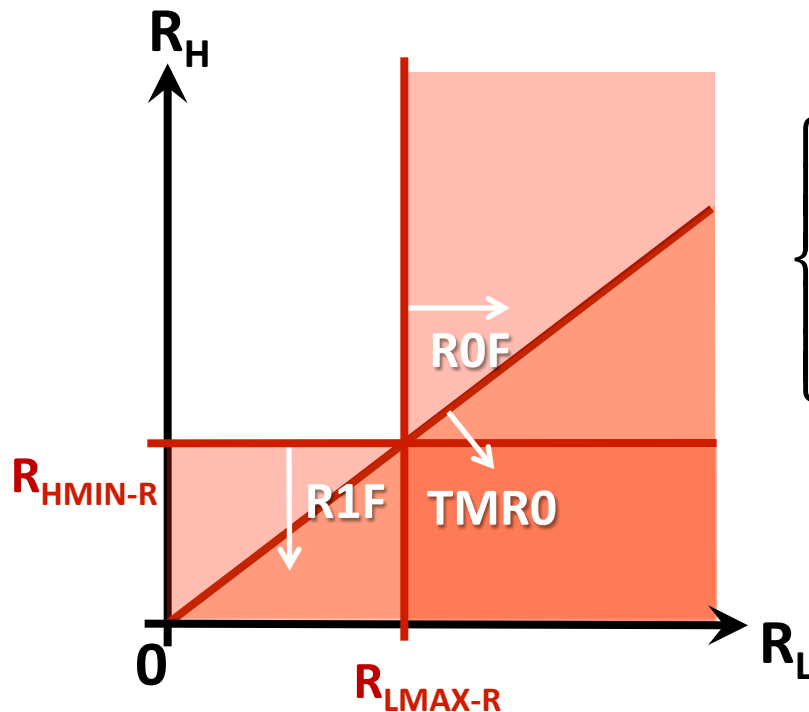
STT MRAM Cell Failure Mechanisms

- Failure during Write Operation (WF)



STT MRAM Cell Failure Mechanisms

- Failure during Read Operation



$$\left\{ \begin{array}{l} R_H > R_{HMIN-R} = \frac{V_{MTJ}}{I_{REF}} = \frac{(V_{BL} - V_{SL})_R}{I_{REF}} - R_{NMOS-R} \\ R_L < R_{LMAX-R} = \frac{V_{MTJ}}{I_{REF}} = \frac{(V_{BL} - V_{BL})_R}{I_{REF}} - R_{NMOS-R} \end{array} \right.$$

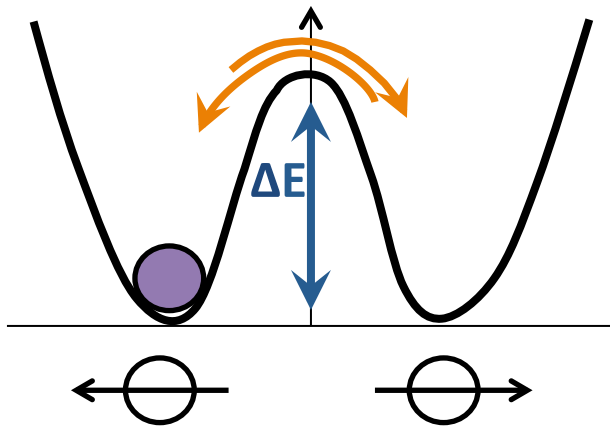
$$I_{REF} = \frac{I_{RH} + I_{RL}}{2}$$

$$R_L < R_{LMAX-R} = R_{HMIN-R} < R_H$$

STT MRAM Cell Failure Mechanisms

- STT-MRAM Cell Failure Probability in Data Retention

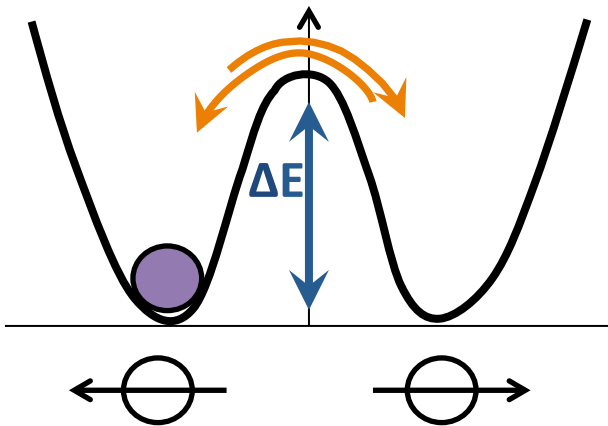
$$P(t) = 1 - \exp[(-Nt/\tau_0) \cdot \exp(-\Delta E/k_B T)]$$



STT MRAM Cell Failure Mechanisms

- STT-MRAM Cell Failure Probability in Read Operation

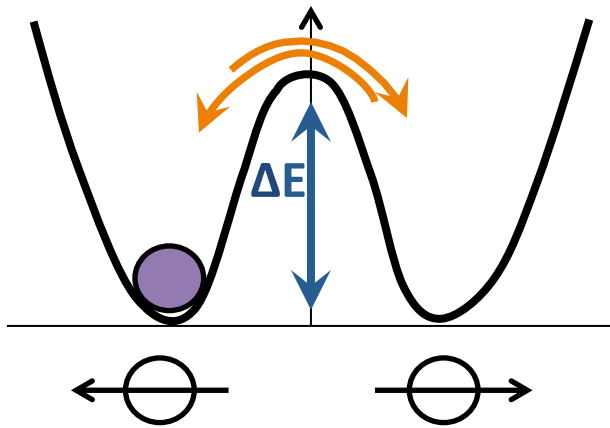
$$P(t) = 1 - \exp[(-Nt/\tau_0) \cdot \exp(-\Delta E(1 - (I_{read}/I_{OC}))/k_B T)]$$



STT MRAM Cell Failure Mechanisms

- STT-MRAM Cell Failure Probability in Write Operation

$$P(t) = \exp[(-Nt/\tau_0) \cdot \exp(-\Delta E(1 - (I_{\text{write}}/I_{\text{OC}}))/k_B T)]$$

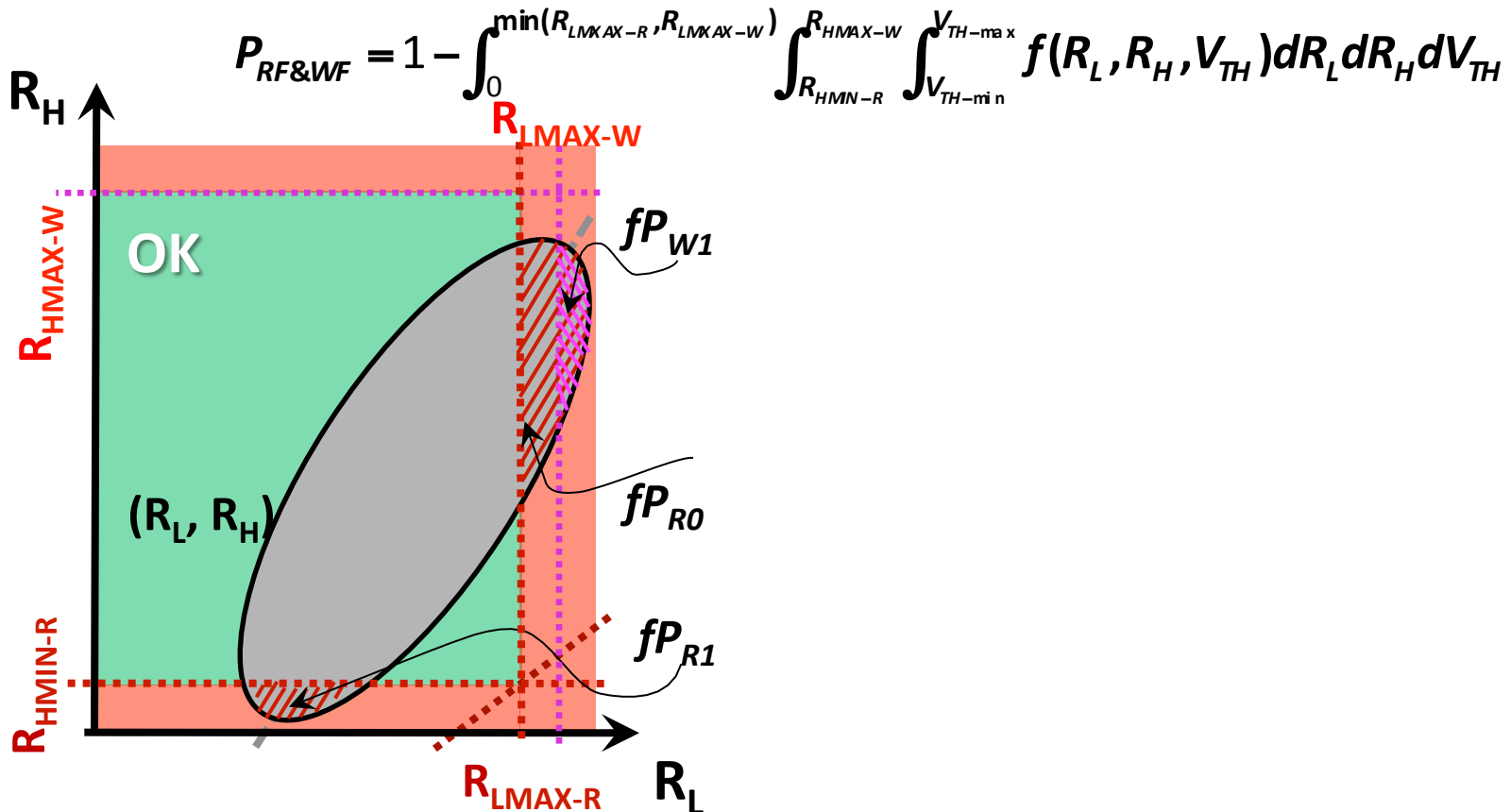


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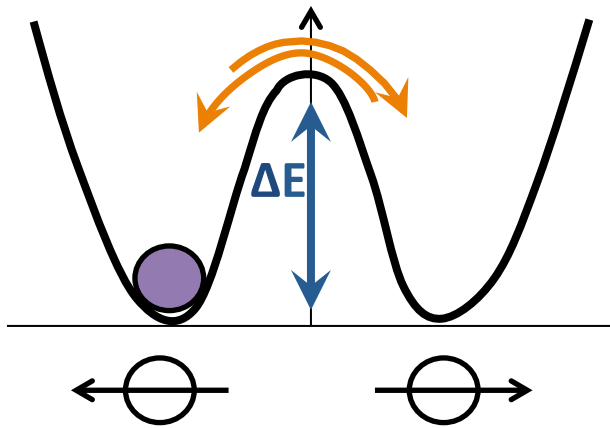
STT MRAM Cell Failure Probability

- STT-MRAM Cell Failure Probability



STT MRAM Cell Failure Probability

- STT-MRAM Cell Failure Probability in Data Retention

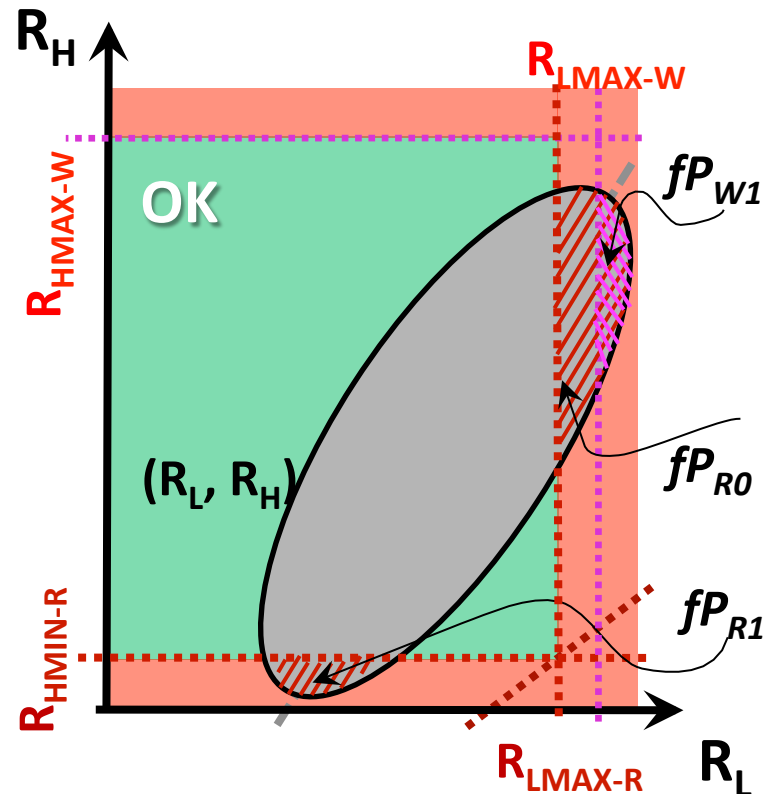
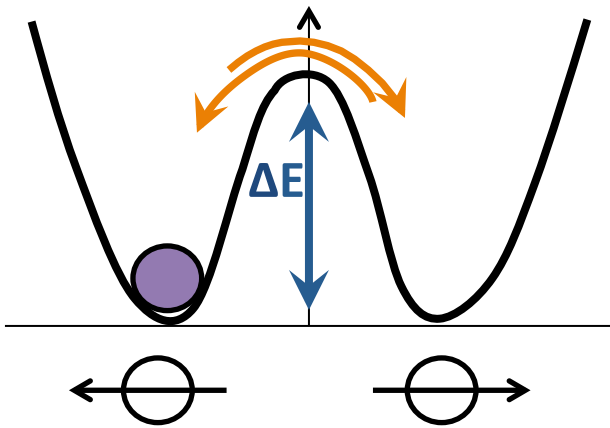


$$P(t) = 1 - \exp[(-Nt/\tau_0) \cdot \exp(-\Delta E/k_B T)]$$

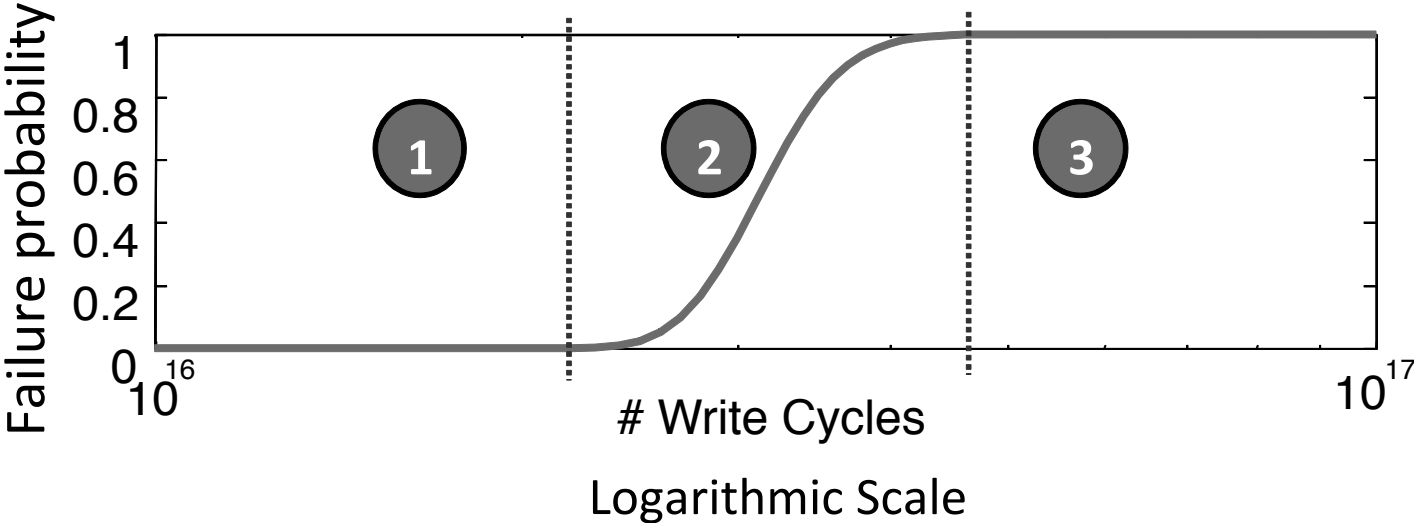
STT MRAM Robustness Probability

- STT-MRAM Cell Failure Probability

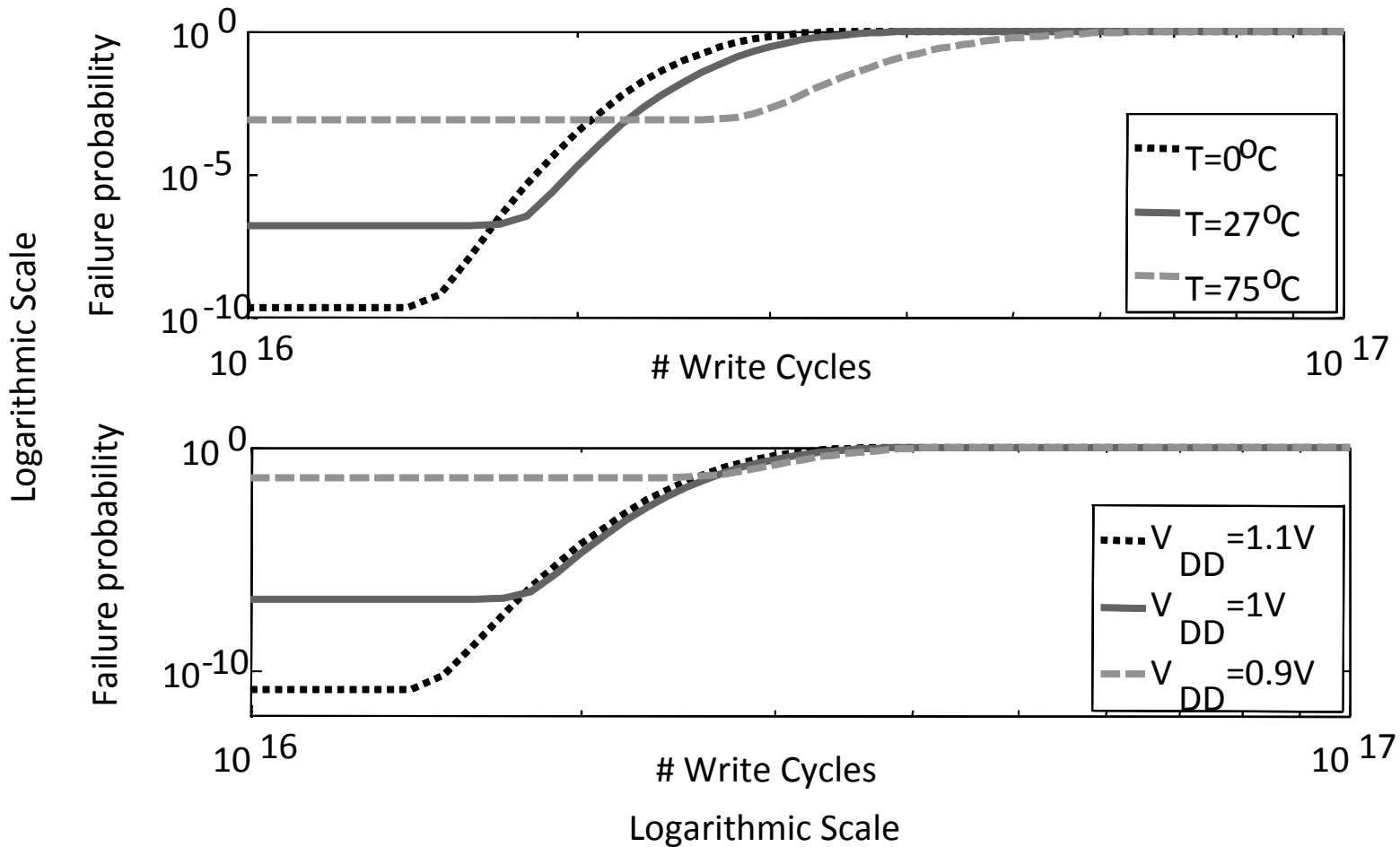
$$P_f = 1 - (1 - P_{RF\&WF}) \cdot (1 - P_{DRF})$$



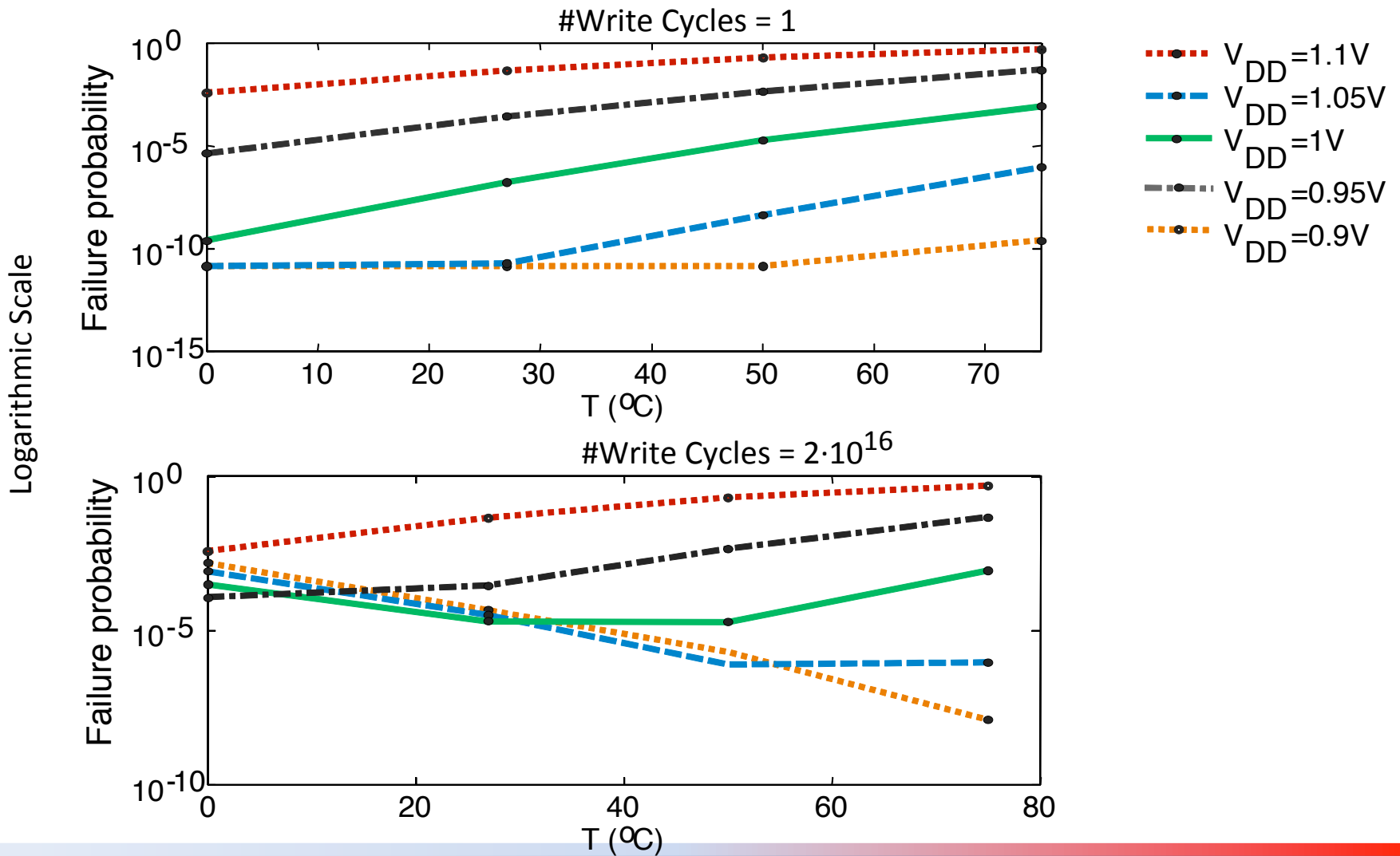
STT MRAM Cell Failure Probability



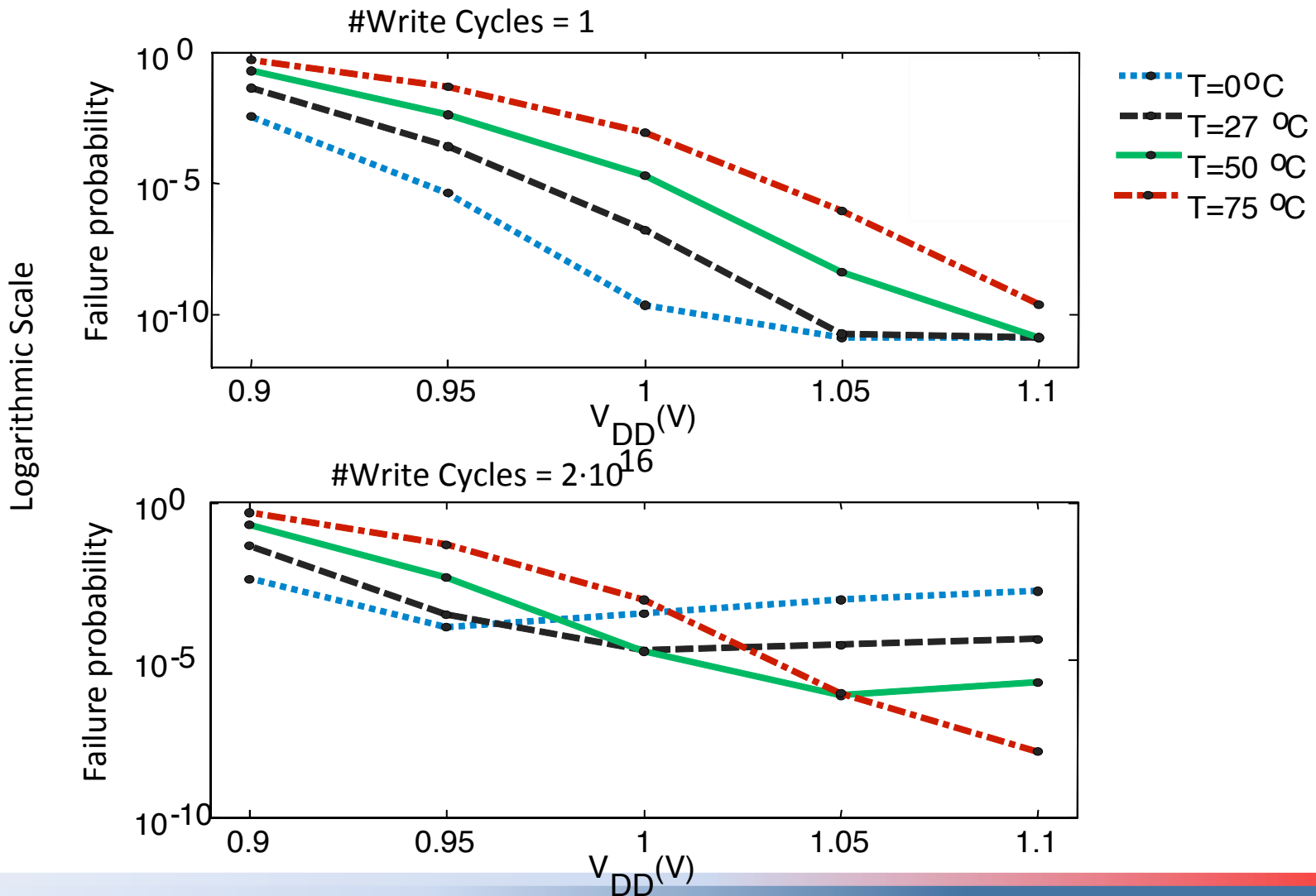
STT MRAM Cell Failure Probability



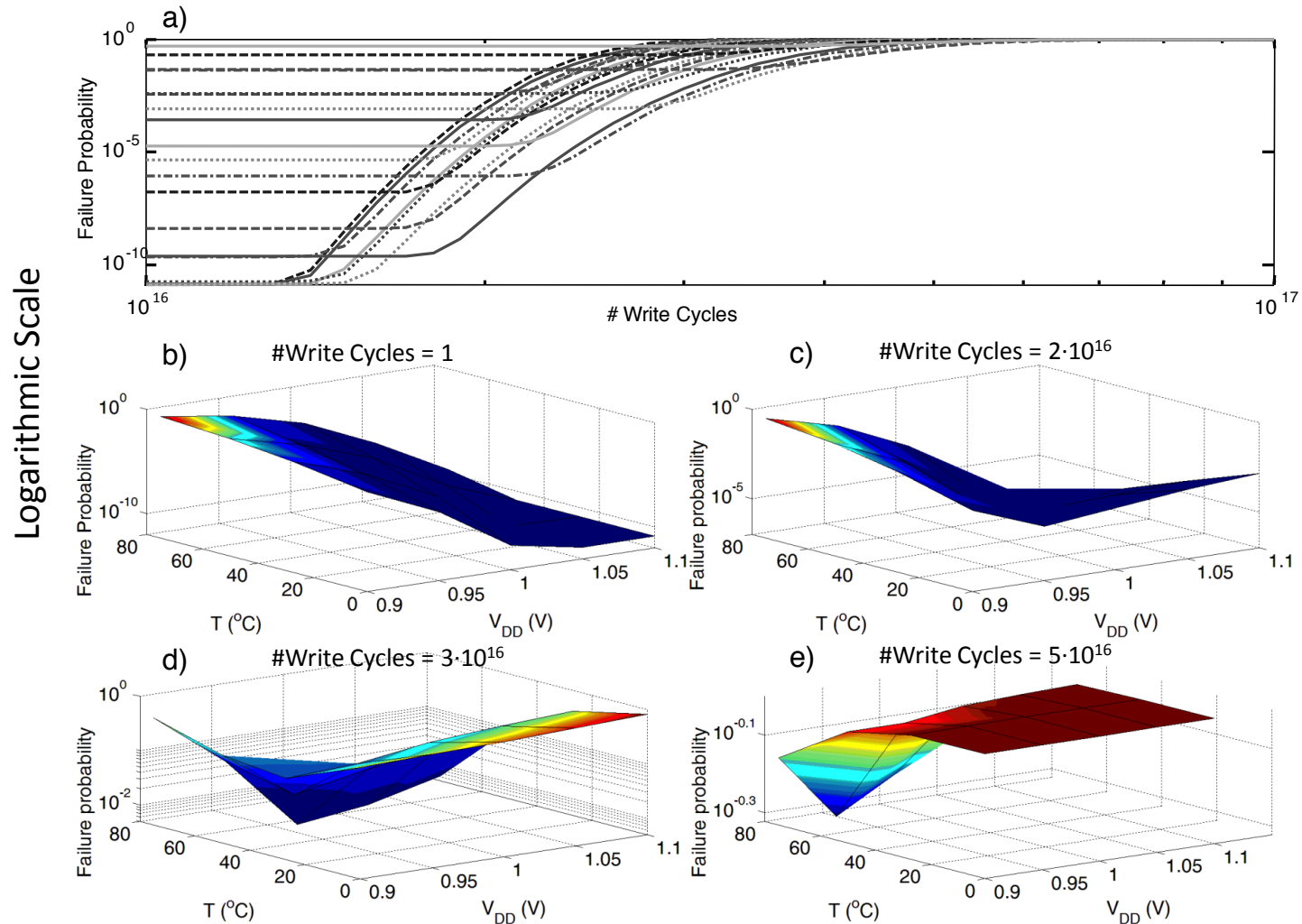
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STT MRAM Cell Failure Probability



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Conclusions

- methodology for STT-MRAM cell reliability prediction
- the joint effect of
 - fabrication- and aging-induced process variability
 - supply voltage variations
 - temperature variations