Impact Objectives

- Develop early and accurate evaluations of the reliability of an electronic system
- Support the development of scaled electronic systems

Rethinking reliability evaluation within electronic systems

Dr Stefano Di Carlo of the Department of Control and Computer Engineering at the Polytechnic of Turin is Coordinator of the CLERECO project, and below he discusses the importance of accurate reliability evaluation within the emerging computing continuum

First, can you briefly outline the overall focus of the CLERECO project?

CLERECO (Cross Layer Early Reliability Evaluation for the Computing cOntinuum) is an electronic design automation (EDA) project. Instead of delivering a product such as a computer, an operating system or application software, we produce software tools to be used by the designers of complex electronic systems. The project focuses on the digital portion of a complex system and thus analogue devices are outside the scope of our project.

Can you explain what Bayesian networks are and describe their novel use within your research?

Bayesian networks are a well-known statistical model for performing statistical reasoning on the causes and effects of stochastic events. When discussing system reliability in relation to hardware faults, Markov models have traditionally been used. Prior to this project, Bayesian models have largely been used in the software reliability field. Software reliability is also an important factor, but it differs from reliability in relation to hardware faults. Software reliability reflects the software design perfection, while in CLERECO we focus on modelling the system behaviour in the presence of faults. In this sense our usage of Bayesian networks is quite novel. In addition to applying the concept within a new area the team has also improved traditional Bayesian networks with new concepts. These concepts are devoted to specifically modelling the different layers composing a complex digital system that include the technology, the hardware architecture and the executed software.

The Bayesian model is a key element of the work done. However, this model is multifarious and cannot be constructed extemporaneously. Without the availability of dedicated tools, the idea of the Bayesian model for a traditional designer would remain a theoretical exercise. Within CLERECO a great deal of work has taken place to design such tools which bridge the gap between theory and practice. Microarchitectural models of the hardware architecture and virtualised software models are two of the main examples of the concepts we integrated in our tools to support the development of our Bayesian model.

What are the consequences of false negatives or false positives in the CLERECO method and do they present a risk?

There is a clear difference in occurrence rates between the two, however the CLERECO project aims to minimise both types. We define a false positive as a system whose reliability is underestimated since the actual probability of fault would be lower than its estimated value and conversely a false negative as a system whose reliability is overestimated. False positives ultimately do not risk the safety and stability of the system but result in over-design and so would waste resources in order to reach the desired reliability level. With a false negative the underestimation of a problem could result in serious consequences for the operation and usability of the system. In comparing the risks of false positive and false negatives it is clear that false negatives need to be avoided and in our work we strive to follow this philosophy.

The key point is that the CLERECO tools are designed to provide rapid reliability estimation during the initial part of the design stage to aid decision-making. The tools do not substitute all tests required for a prototyped system when assessing its final reliability. Accordingly, in both cases the risks would impact the need to redesign the system due to the fact that the final reliability level is different from the one estimated in the early phases.

Why is CLERECO important at the design stage?

Our tools help designers understand how a technology, hardware architecture and application software work together in a complex system. This results in an understanding of the system's reaction to sources of failure which arise during work in the field. Advanced knowledge of the threats a system will encounter during its lifetime allows the designer to appropriately allocate the countermeasures implemented and ensure these threats will not impact upon the safety of the users. This challenge of implementing fault tolerance is a key area of cost in terms of system performance, energy consumption, component size and design time.

Design for reliability in the era of the computing continuum

*The **CLERECO** collaborative project proposes a scalable, cross-layer methodology and supporting suite of tools for accurate and fast estimations of computing systems' reliability*

As we enter the era of nanoscale devices, reliability is becoming a key challenge for the semiconductor industry. The now atomic dimensions of transistors result in a vulnerability to variations in the manufacturing process and can dramatically increase the effect of environmental stress on the correct circuit behaviour. Failures in early assessing computing systems' reliability may produce excessive redesign costs which can have severe consequences for the success of a product.

Current practice involves a worst-case design approach with large guard bands. Unfortunately, application of this approach is reaching its limit in terms of economic sustainability with regard to performance, size and energy costs. Coordinated by Dr Stefano Di Carlo of the Polytechnic of Turin, the CLERECO (Cross Layer Early Reliability Evaluation for the Computing cOntinuum) project aims to address this challenge.

The CLERECO project involves industrial and academic partnerships between four academic institutions and three manufacturers in order to create a new approach and new tools for electronic design automation (EDA) support in reliability assessment. The project addresses a key challenge faced by designers employing measures to prevent hardware faults propagating to the software layers of the system stack and reaching the system output. Different protection mechanisms must be employed at each layer in order to provide 'cross-layer' reliability enhancement. This challenge becomes more serious when coupled with the concept of the 'computing continuum'. This phrase was coined by Intel in 2011 and describes the erosion of the traditional separation between the market segments of embedded systems and high performance computing systems. CLERECO aims to reflect this merging of market segments at the EDA level by providing tools that can be applied with small differences to different computer architectures and across a range of areas. CLERECO has been in operation since 2013, with key milestones including theoretical models, tool design, adaptation of tools for industry use, and commercialisation of the created tools by partner organisations.

A NEW METHODOLOGY AND APPROACH

The CLERECO project focuses on reliability analysis in the early phases of the design. Early assessment within the design cycle provides the freedom for adaptive modification if the estimated reliability level does not meet the requirements. Traditional tests typically take place at the end of the design stage when a prototype of the system is available. Physical stress tests are generally used to evaluate the final reliability of a system. When working with models of the design, register transfer level or gate-level fault injection (FI) is the most accurate standard method for performing reliability analysis. The designer creates a detailed model of the system hardware and is able to simulate the execution of software applications on this model. To perform reliability analysis, faults are artificially injected into the model, thus simulating what could happen in a real environment, and the effect of the faults are evaluated by comparing the behaviour of the faulty system with a fault-free version. Theoretically, by performing a statistically significant number of simulations a very precise estimation of the reliability of the system can be identified.

Di Carlo identifies problems with this approach: 'These detailed gate-level models, especially for complex hardware blocks such as microprocessors are not always available, and the simulation time in case of complex systems is prohibitive. Usually this results in the use of simplified simulations and models.' This leads, in Di Carlo's opinion, to 'inaccurate and usually pessimistic estimations'. CLERECO methodology addresses this challenge by providing dedicated tools to separately analyse the technology, the hardware components (at the microarchitecture level) and the software modules of a complex system and to recombine the characteristics of single objects into a complex statistical Bayesian model. This can be used to perform statistical reasoning on the reliability of the system as a whole.

As part of the project a comparative analysis was undertaken to compare reliability estimations gathered using the CLERECO tools with those obtained using an accurate and a simplified gate-level fault injection campaign. The results revealed an equivalent level of estimated reliability, with a significant reduction in simulation time required when using a CLERECO reliability estimation approach versus an industry standard gate-level FI campaign.

INDUSTRIAL CHALLENGES

Di Carlo describes several challenges faced during the project in relation to the stability of the industrial team: 'Within three years there were three changes in the composition of the industrial consortium. Intel Corporation Iberia SA (Spain) left the consortium after eight months due to closure of the local facility; similarly, after 18 months ABB AS (Norway) left due to closure of the local facility and ABB activities moved to ABB AB (Sweden). Finally, Yogitech SpA was acquired by Intel at the end of the project, producing another change and bringing Intel Corporation Italia SpA in the consortium.'

The project remained intact but the turbulence created by such changes

“The complexity of the new technologies requires a deeper collaboration between industry and academia. We could not have achieved our results without the strong support of our industrial partners”

represented a significant overhead for Di Carlo and, in some cases, represented a threat to the continuation of the project. The ability to weather such turbulence relied on the effective backup plans for these situations and on the research strength and dedication of the academic partners which guaranteed the smooth continuation and the successful completion of the project.

This instability of the industrial consortium is not unique to the CLERECO project, however. The current situation within the global economy, as well as the speed at which IT business changes, makes a three-year commitment in a research project increasingly difficult for industrial partners. In contrast to this, Di Carlo explains, ‘There were few major scientific challenges and there was a good and very productive collaboration among all partners.’

MARKET-READY RESULTS

Industrial partners have been very important during the project despite the changes mentioned above. CLERECO worked in collaboration to build tools that could be inserted directly into industrial design flows. As Di Carlo outlines, ‘There are so many academic tools around that don’t find real application in the industry since they are not built to be integrated into a real industrial design flow.’ Industrial partners, provided guidelines on the use of tools and models, thus creating a key area of value for the project. Di Carlo notes that the ‘complexity of the new technologies requires a deeper collaboration between industry and academia. We could not have achieved our results without the strong support of our industrial partners’.

Industrial partners also provided systems on which the tools and models were tested. Benchmarks are effective instruments for evaluation of the capability of a tool but only when working with real cases can the practical limits of an approach be understood. This academic and industrial partnership allowed a move from laboratory-based benchmark analysis to real systems in order to identify system-based bottlenecks. These have now been corrected, allowing delivery of mature products.

Industrial partners also provided the tools and knowledge to perform a fair comparison of CLERECO methods with existing gold standard commercial products. In particular, Yogitech SpA had already commercialised products for reliability analysis based on gate-level FI. Due to the contribution of Yogitech it was possible to compare the CLERECO early reliability estimation tools with a commercial reliability analysis workflow, showing how early reliability analysis can complement precise FI-based validation at the end of the design flow.

SHARING KNOWLEDGE

CLERECO partners also provide a channel for exploitation and presentation of the project’s results. In 2016 alone the CLERECO team has presented at the Institute of Electrical and Electronics (IEEE) Engineers ITC (International Test Conference) in Dallas, HiPEAC Conference, DATE (Design Automation and Test in Europe), ISPASS (International Symposium on Performance Analysis of Systems and Software), VTS (IEEE VLSI Test Symposium), ICCD (IEEE International Conference on Computer Design), IOLTS (IEEE International Symposium on On-Line Testing and Robust System Design), PATMOS (International Workshop on Power And Timing Modeling, Optimization and Simulation), DCIS (Design of Circuits and Integrated Systems Conference) and CTC (China Test Conference).

Project Insights

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