MaFIN

Clereco
Cross-Layer Early Reliability Evaluation for the Computing cOntinuum

FP7-CLERECO
Grant Agreement FP7-611404
SEVENTH FRAMEWORK PROGRAMME

Microarchitecture Level Fault Injector for x86 Intel/AMD CPUs

March 2016

Product overview

MaFIN is a complete microarchitecture level reliability evaluation framework for high performance computing systems. It is based on state-of-the-art statistical fault injection method or ACE analysis and built on MARSSx86 full-system simulator, providing accurate results for the entire CPU and all its components.

"Fast microarchitecture level framework for Intel/AMD x86-64 early reliability assessments"

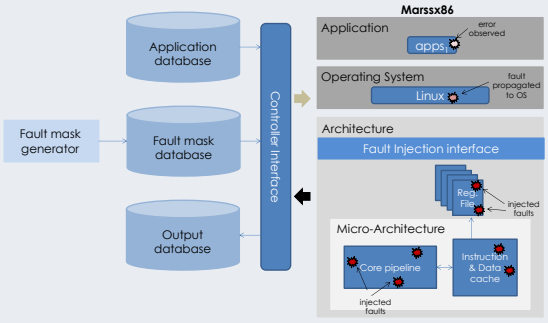
- Computer Architecture Lab
University of Athens

Supported Architectures

⇒ **Embedded and high performance x86-64 Intel and AMD** architectures

Extensions & Tools

- Caches extended with the data field (L1 data, L1 instruction and unified L2 cache)
- Prefetchers added for the first level caches
- **Fully automated** tools for:
  1. running the golden run
  2. fault mask generation
  3. fault injection in MARSSx86
  4. Faults classification



Target Components

- Physical Register File (Int, FP)
- All fields of caches (L1 data and instruction, L2, L3)
- Prefetchers of L1 data, L1 instruction
- Load/Store Queue
- Load/Store Aliasing Table
- Issue Queue
- Branch Prediction Unit, RAS, BTBs

Supported Fault Models

⇒ **Transient**
⇒ **Intermittent**
⇒ **Permanent**

} any multiple combination of model, component, entry and cycle

Measurements

- **AVF/FIT, HVF**
- **Fault effect classification:**
  1. **Masked**
  2. **Silent Data Corruption (SDC)**
  3. **Crash**
  4. **Assert**
  5. **Timeout**
  6. **DUE**

Flexible user extensible parser.

*Measurements in **any unmodified workload**.*

Speedup Features

Speedup of fault injection campaigns is based on two runtime modes:

- **Early Stop on Overwrite (ESO mode)**:
  - ⇒ No loss of accuracy
  - ⇒ Speedup:
    - 2.6X for integer register file
    - 1.5X for LSQ (data field)
    - 2.9X for LSQ (address field)
    - 1.4X for L1 data cache
    - 1.5X for L1 instruction cache
- **Early Stop on Overwrite or first Read (ESOR mode)**:
  - ⇒ Negligible loss of accuracy for structures in the core
  - ⇒ Speedup:
    - 3.4X for integer register file
    - 3.4X for LSQ (data field)
    - 4.1X for LSQ (address field)
    - 2.1X for L1 data cache
    - 1.8X for L1 instruction cache

https://twitter.com/CalDiUoa

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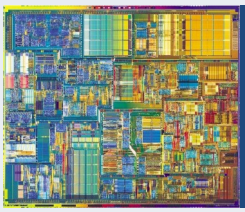

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