SERTA

Clereco
Cross-Layer Early Reliability Evaluation for the Computing cOntinuum

FP7-CLERECO
Grant Agreement FP7-611404

SEVENTH FRAMEWORK PROGRAMME

Soft Error Rate Technology Analyzer — **March 2016**

Product Overview

SERTA (SER Technology Analyzer) allows for a fast characterization of raw failure rates of current and future technologies for a variety of components such as memories (i.e. SRAMs) and the most common logic gates (i.e. NAND, NOR, NOT). It also provide a sensitivity analysis to operating conditions such as temperature, voltage and location.

*"Technology reliability is not only about the **present**, it is about the **future** too"*

- ARCO Research Group (UPC)

Supported Architectures

- Any technology based on SPICE description

Target Components

- Memories
- Logic Gates

Extensions & Tools

- Compliant with the Hazucha and Svensson model
- Fully parametrized analysis.
- Full Technology fair comparison available

Supported Fault Models

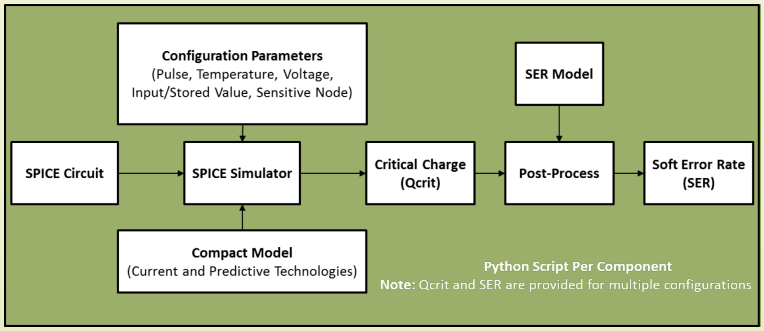
✓ **Soft Errors**

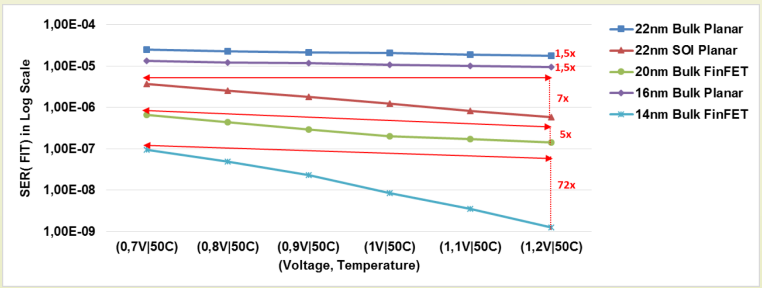
Measurements

- SER value across several environmental conditions

Extra Features

- The tool also allows to perform a fair comparison of these technologies and components using the same methodology to compute their SER.





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