Clereco
Cross-Layer Early Reliability Evaluation for the Computing cOntinuum

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SEVENTH FRAMEWORK PROGRAMME

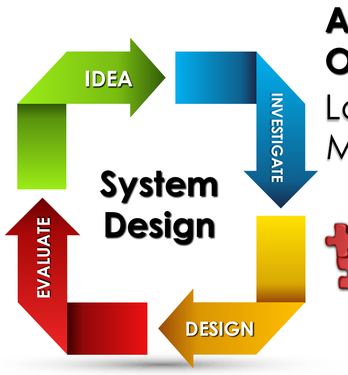
# Cross-Layer Reliability

Error management at different design layers: **technology**, **hardware**, **software.**


**What's the best combination?**

Fault Injection
Physical stress test

Reliability engineers and system architects are required to fulfill demanding safety requirements to budget and to allocate reliability targets per system component while depending on incomplete or missing reliability data

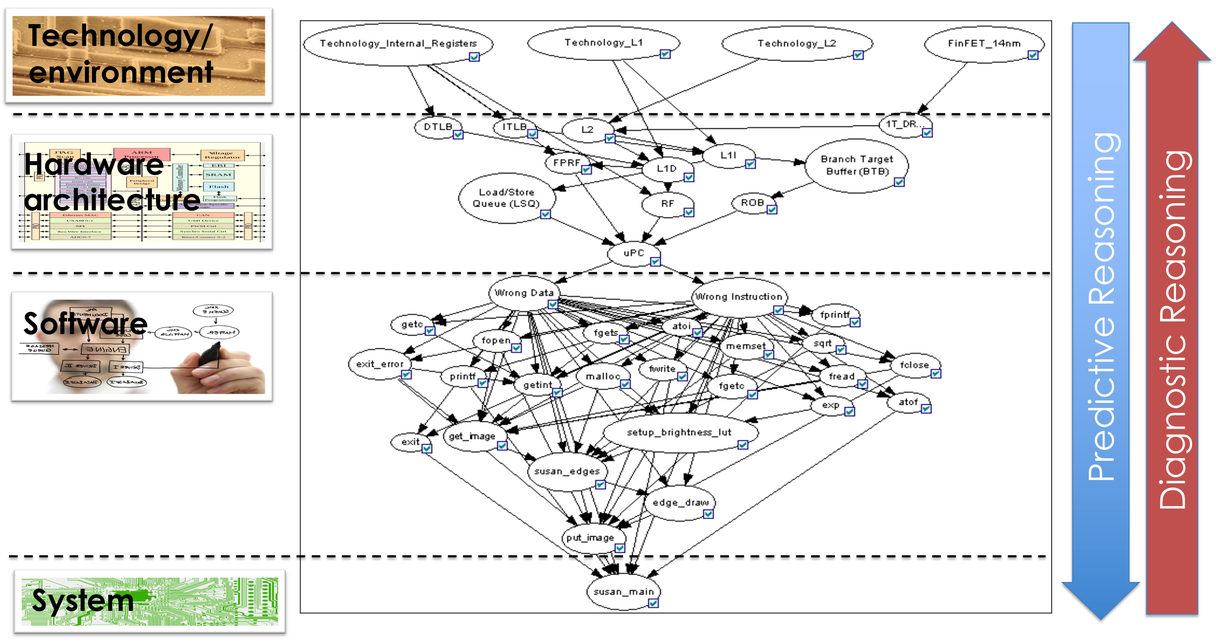



**A safe approach: OVERDESIGN**
Large margins
Massive redundancy

**Reliability Costs**


**Can tools to evaluate reliability early in the design help designing more efficient systems?**

# System Reliability Analyzer



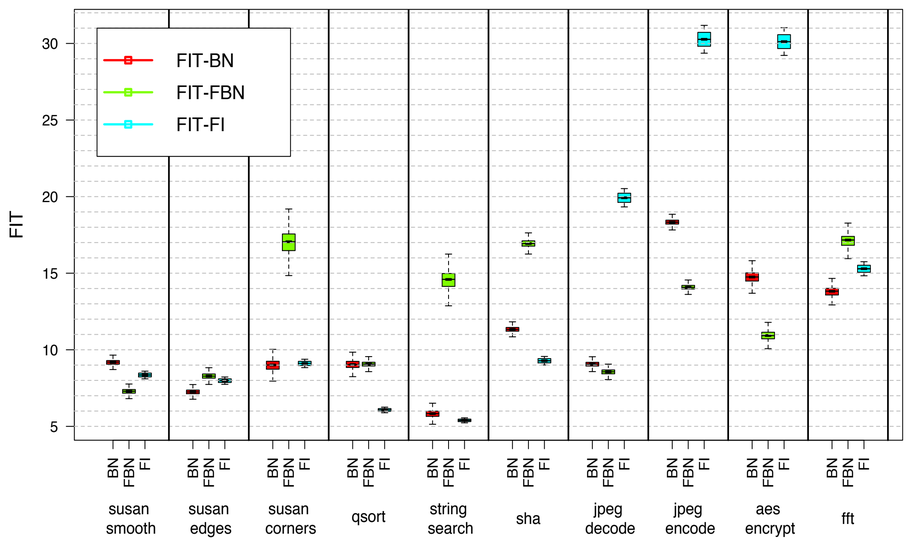

**Component-Based Bayesian Network (BN) reliability model**

- Nodes represent HW/SW system's components.
- Edges represent error masking/propagation paths within the system
- Masking probability computed through our library of dedicated tools

**Reasoning:**

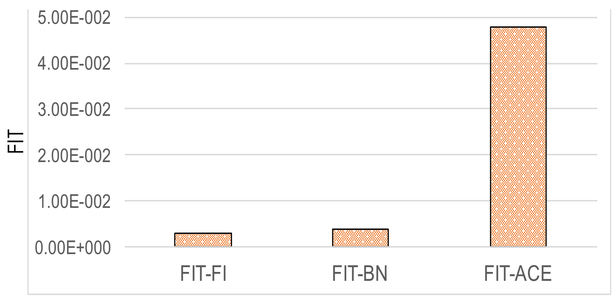
- **Diagnostic** from symptoms (i.e., system failures) we update our belief about causes of failures.
- **Predictive** from causes (i.e., raw technology failure rates) we obtain new beliefs about their effects (i.e., system failures).

**Some results:**

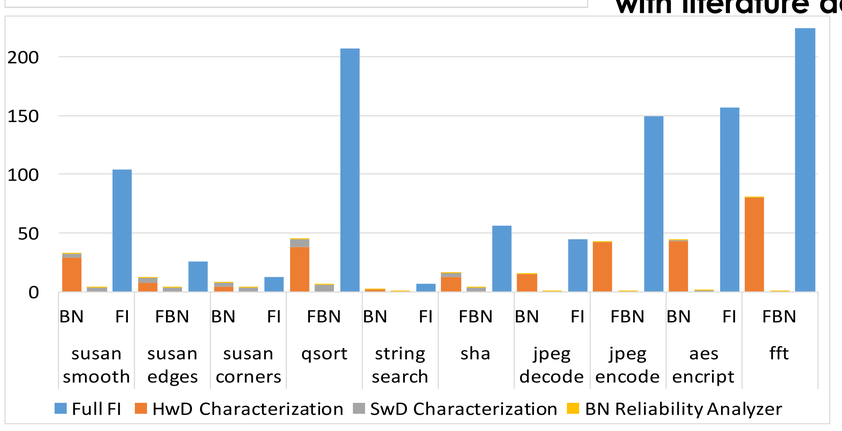



**Technology:** 22nm Bulk Planar
**Hardware architecture:** x86 *out-of-order CPU*
Register file (256 regs each 64-bits)
32KB L1 Instruction Cache
32KB L2 Data Cache
1MB L2 Cache
128 B Load/Store Queue
4GB ECC Protected DRAM

**FIT estimation for a x86 based system running 10 software benchmarks: (1) $FIT_{BN}$ computed with the CLERECO model, (2) $FIT_{FBN}$ computed with the CLERECO model using average masking probabilities, (3) $FIT_{FI}$ computed using full fault injection campaigns**



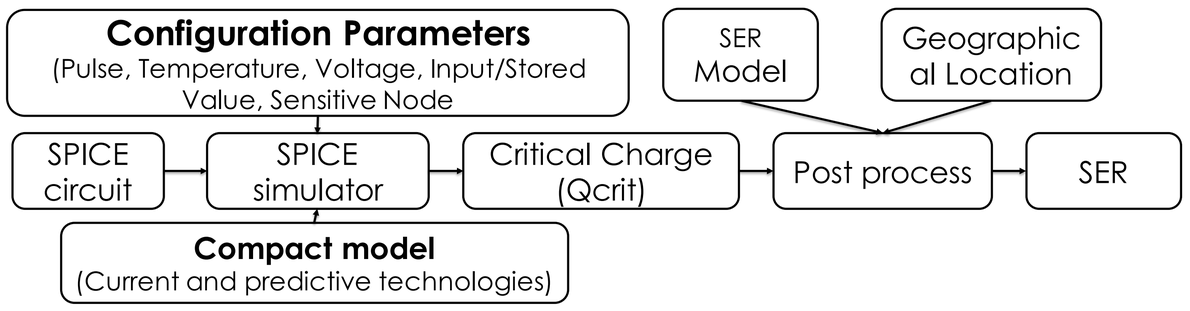

**Comparison with AVF computed through ACE analysis for the string search benchmark computed with technology: $FIT_{BN}$ computed with the CLERECO model, $FIT_{FI}$ computed using full fault injection campaigns, $FIT_{ACE}$ computed using ACE analysis with literature data**




**Simulation time comparison in hours of simulation:**
**BN: CLERECO Bayesian Reliability Analyzer**
**FI: full micro architectural level fault injection campaign.**

# Technology/Environment Analyzer

Soft-errors characterization tool suite for different technologies and basic building blocks




**CLERECO Tech. Library**

| Technology (CMOS) | Technology node |
|---|---|
| Bulk Planar (ASU PTM Models) | 22nm and 16nm |
| Bulk FinFET (ASU PTM Models) | 20nm and 14nm |
| SOI Planar (UTSOI Model) | 22nm |

X

| Circuits |
|---|
| SRAM Cells 6T/8T/10T |
| Flip Flop - D |
| Latch |
| Logic Gates |

# Hardware Vulnerability Analysis

Tool suite to characterize hardware vulnerability to faults for different categories of components

- Transient, intermittent and permanent faults, targeting one or multi bits at one or more components.
- Analysis based on:
  - Analytical models
  - Statistical fault injection based on architectural models

**CPUs**
x86-64 OoO model
(general x86, x86-64 ISA support)
ARM OoO A9/A15 models
(general ARM ISA support)

**GPUs**
NVIDIA G80, GT200 and Fermi,
AMD Southern Island, Evergreen

**Memories**
SRAM, DRAM,
SSD (NAND Flash, STT MRAM)

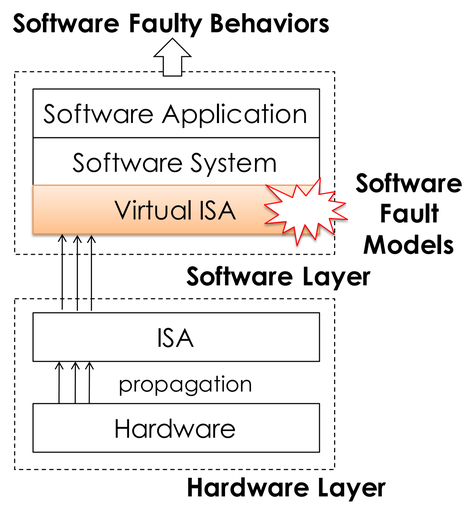
**Custom cores and peripherals**

**Interconnections**
AMBA, PCI Express, NoCs

# Software Vulnerability Analyzer

**Virtual ISA-based Fault Injection**

- **Virtual ISA:** LLVM (A framework that uses virtualization to perform complex analysis of software applications on different architectures)
- **Fault models**: Software Fault Model (Effect of soft errors on the virtual ISA)




| Fault Model | Description |
|---|---|
| Wrong Data in an Operand | An operand of the VISA instruction changes its value |
| Not accessible Operand | An Operand of the VISA instruction cannot change its value |
| Instruction Replacement | An instruction is used in place of another |
| Control Flow Error | The Control Flow is not respected |

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